


FPGA 原型验证平台测试报告及功能参数 佐证材料

上海合见工业软件集团有限公司

2023 年 1 月



1、FPGA原型验证平台：UV-19P-Q平台，核心芯片选用XilinxXCVU19P，芯片工艺16nm。

Product Advantages	Application	Product Table	Documentation	Get Started	Video
		<p>Virtex™ UltraScale+™ devices provide the highest performance and integration capabilities in a 14nm/16nm FinFET node. AMD 3rd generation 3D ICs use stacked silicon interconnect (SSI) technology to break through the limitations of Moore's law and deliver the highest signal processing and serial I/O bandwidth to satisfy the most demanding design requirements. It also provides registered inter-die routing lines enabling >600 MHz operation, with abundant and flexible clocking to deliver a virtual monolithic design experience.</p> <p>As the industry's most capable FPGA family, the devices are ideal for compute-intensive applications ranging from 1+Tb/s networking, machine learning, to radar/early-warning systems.</p>			

2、FPGA原型验证平台：UV-19P-Q平台板载4颗芯片，单颗芯片逻辑资源9M，四颗芯片资源36M。

<https://docs.xilinx.com/v/u/en-US/ultrascale-plus-fpga-product-selection-guide>

[illegible]

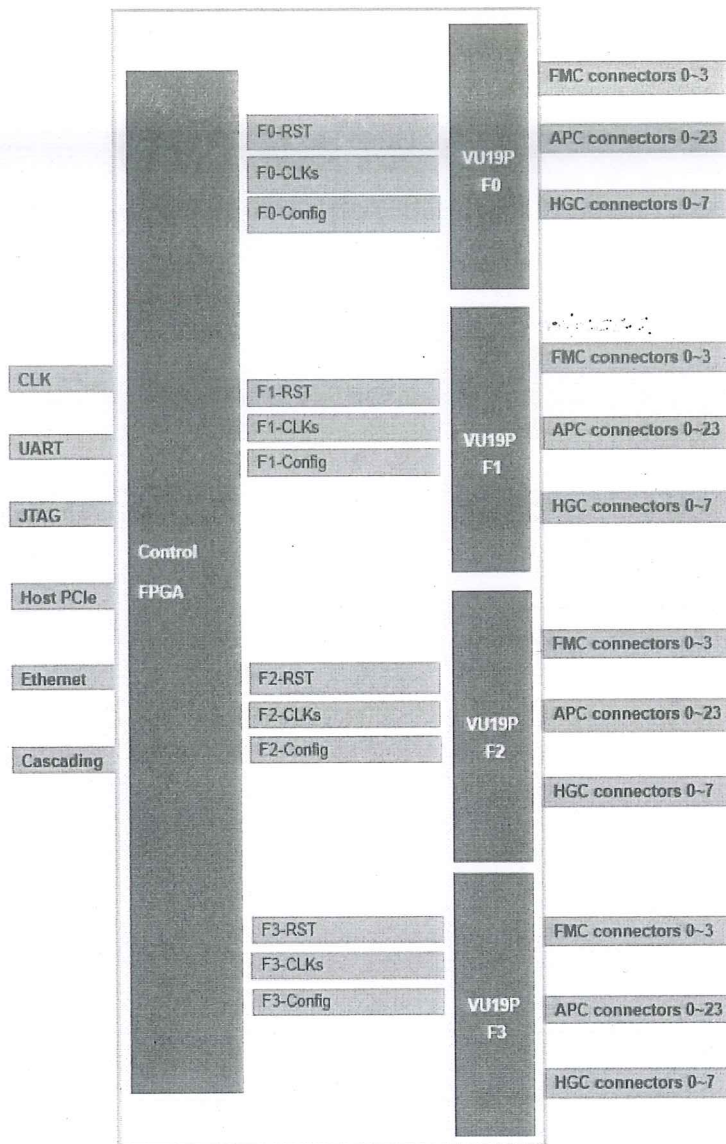


Figure 2-1 Functional block diagram of the UV APS

3、FPGA原型验证平台：UV-19P-Q平台，单颗芯片RAM资源165Mbit，四颗芯片资源660Mbit。

佐证材料：详见Xilinx VU+系列FPGA产品手册p3页

Foundation											800 PAM4		
Device Name	VU19P	VU19P	VU19P	VU19P	VU19P	VU19P	VU19P	VU23P	VU27P	VU29P			
System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	8,838	2,252	2,885	3,780			
Logic PIPs (K)	786	1,201	1,576	2,481	2,730	3,675	8,838	2,252	2,885	3,780			
Configurable Logic Blocks (K)	394	601	785	1,182	1,290	1,735	4,085	1,030	1,290	1,735			
Max. Dual RAM (Mb)	12.0	18.3	24.1	36.1	36.7	48.3	58.4	14.7	16.7	48.3			
Total Block RAM (Mb)	25.1	36.0	50.6	75.9	75.9	94.5	75.9	74.9	70.9	94.5			
Block RAM (Mb)	55.6	132.1	169.6	270.0	270.0	360.0	360.0	99.0	270.0	360.0			
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	3,840	1,120	9,216	12,288			
Peak INTL DSP (TOP/s)	7.1	10.5	14.2	21.5	28.7	38.3	10.4	4.1	28.7	38.3			
PCIe Gen3 x16 (TDP/s)	2	4	4	6	5	4	6	0	1	1			
PCIe Gen3 x16 (TDP/s) / CDP ¹⁾	2	4	4	6	5	4	6	0	1	1			
100Gb Ethernet w/ 8x8 RS-FEC	3	4	6	9	6	8	0	0	5	8			
Max. Single-Ended HP VIOs	512	832	832	832	832	832	1,976	572	676	676			
Max. Single-Ended HD VIOs	0	0	0	0	0	0	56	72	0	0			
GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	80	34	32	32			
GTY 58Gb/s PAM4 Transceivers	—	—	—	—	—	—	—	6	48	48			
100G/500G PAM4 FEC	—	—	—	—	—	—	—	2/4	24/48	24/48			
Extended ¹⁾	-1-2-21-3	-1-2-21-3	-1-2-21-3	-1-2-21-3	-1-2-21-3	-1-2-21-3	-1-2	-1-2-21-3	-1-2-21-3	-1-2-21-3			
Industrial ²⁾	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2			
Footprint 14.1	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 102 671						FF 102 102 671						
Dimensions	FF 10												

Device Name	Foundation							SAG PPA4		
	UV1P	UV1P	UV1P	UV1P	UV1P	UV1P	UV1P	UV23F	UV23F	UV23F
System Logic Cells (K)	852	1,314	1,724	2,586	2,835	3,740	8,838	2,232	2,885	3,780
Logic PIPs (K)	797	1,261	1,671	2,533	2,782	3,687	8,777	2,159	2,812	3,707
CLB LUTs (K)	394	625	786	1,142	1,266	1,712	4,088	1,030	1,290	1,723
Max. Dist. RAM (Mm)	12.0	18.3	24.1	36.1	36.2	48.3	98.4	14.7	16.3	18.3
Total Block RAM (Mm)	25.3	36.0	50.9	75.9	70.9	94.5	75.9	74.3	70.9	94.5
UltraRAM (Mm)	15.0	13.2	16.0	27.0	27.0	36.0	60.0	99.6	77.0	100.0
DSP Slices	2,280	3,474	4,560	6,840	7,216	9,288	2,840	1,820	2,216	2,888
Peak INTS DSP (TOP/s)	7.1	10.8	14.2	21.3	22.7	28.3	10.4	4.1	20.7	30.3
PCIe Gen3 x16 (TOP/s)	2	4	4	6	5	8	8	6	1	1
PCIe Gen3 x16 (TOP/s) / (TOP/s)	—	—	—	—	—	—	—	—	—	—
150G Interconnect	3	4	6	9	6	8	8	8	8	8
100G Ethernet w/ 8B/10B FEC	3	4	6	9	6	8	8	8	8	8
Max. Single-Ended HD U/Ds	512	832	832	832	832	832	1,976	572	676	676
Max. Single-Ended HD U/Ds	0	0	0	0	0	0	86	72	0	0
GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	80	34	32	32
GTY 58.5Gb/s PAM4 Transceivers	—	—	—	—	—	—	—	—	—	—
100G/500G P4 FEC	—	—	—	—	—	—	—	—	—	—
Extended ¹	-1-2, 2L-3	-1-2, 2L-3	-1-2, 2L-3	-1-2, 2L-3	-1-2, 2L-3	-1-2, 2L-3	-1-2	-1-2, 2L-3	-1-2, 2L-3	-1-2, 2L-3
Extended ²	-1-2	-1-2	-1-2	-3-2	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2
Footprint 14.1	Footprint 14.1							Footprint 14.1		
Area (mm ²)	354.37	520.40	—	—	—	—	—	364.9, 364.9	—	—
C1517	40x40	—	—	—	—	—	—	572, 72, 36, 4	—	—
F1824 ³	45x45	—	—	—	—	—	—	—	—	—
A3104	47.5x47.5	832, 52	832, 52	832, 52	—	832, 52	—	—	—	—
E2104	52.5x52.5 ⁴	702, 76	702, 76	702, 76	572, 76	—	—	—	—	—
E2104	52.5x52.5 ⁵	—	—	—	—	702, 76	—	—	—	—
C2104	47.5x47.5	416, 80	416, 80	416, 104	416, 96	—	—	—	—	—
D2104	47.5x47.5	—	—	676, 76	572, 76	416, 104	—	—	—	—
D2104	52.5x52.5 ⁶	—	—	—	—	676, 76	—	676, 36, 80	676, 36, 80	676, 36, 80
H2104	47.5x47.5	—	—	—	—	—	—	—	—	—
A2577	52.5x52.5	—	—	448, 126	448, 96	448, 126	1,976, 86, 48	448, 32, 48	448, 32, 48	448, 32, 48
A3824	65x65	—	—	—	—	—	—	—	—	—
R3824	65x65	—	—	—	—	—	—	—	—	—

6、FPGA原型验证平台：UV-19P-Q平台高速接口速度支持速率25Gbps。

佐证材料：

UVAPS-PM-011-00053-0A_2211 P19

Callout	Component name	Description	Cable
2	HGC0 to HGC7	<p>8 × HGC connectors</p> <p>The 8 HGC connectors provide 32 GTY transceivers in total. They serve to interconnect between XCVU19Ps.</p> <p>Each HGC connector:</p> <ul style="list-style-type: none"> Provides 4 GTY transceivers to support 1 GTY quad of the XCVU19P. Supports up to 28.21 Gbps GTY line rate. 	<p>UV-HGC-</p> <p><length_mm></p>

7、FPGA原型验证平台：UV-19P-Q平台IO电平可支持1.2V, 1.35V, 1.5V, 1.8V。

佐证材料：UVAPS-PM-011-00053-0A_2211 P14

- Connectors on each XCVU19P include:
 - 4 high-pin count FMC connectors to provide 596 IOs and 14 GTY transceivers in total
Each FMC connector supports adjustable voltages from 1.0V to 1.8V.
 - 24 APC connectors to provide 1224 high performance IOs in total
 - 8 HGC connectors to provide 32 GTY transceivers in total

8、FPGA原型验证平台：UV-19P-Q平台支持DDR4输入时钟可编程。

佐证材料：NE-FMCH-PDDR4_HWUserManual_V1.1.1 p10页

2 Overview

UV-FMCH-PDDR4 has 5 DDR4 SDRAM and offers up to 4 GB DDR4 SDRAM memory and can be accessed over a 72bit data bus(ECC). This board can be used with performances of up to 2400 Mbps(on UV-VU19P-CORE board's FMC2 or FMC4 or FMC7 or FMC9). Besides the board offers 8 on board LEDs, which we can used for debug purpose.

3 Feature

◆ FMC Connector	: Samtec's ASP-134488-01
◆ DDR4 SDRAM	: MICRON or Samsung
◆ PROGRAM CLOCK	: Supported
◆ Maximum Speed	: 2400Mbps

9、FPGA原型验证平台：UV-19P-Q平台支持DDR4功能卡, 容量：16G, 接口形式FMC, 速率达到1866Mbps以上，提供DDR4功能卡。

佐证材料：NE-FMCH-PDDR4_HWUserManual_V1.1.1 p10页

2 Overview

UV-FMCH-PDDR4 has 5 DDR4 SDRAM and offers up to 4 GB DDR4 SDRAM memory and can be accessed over a 72bit data bus(ECC). This board can be used with performances of up to 2400 Mbps(on UV-VU19P-CORE board's FMC2 or FMC4 or FMC7 or FMC9). Besides the board offers 8 on board LEDs, which we can used for debug purpose.

3 Feature

◆ FMC Connector	: Samtec's ASP-134488-01
◆ DDR4 SDRAM	: MICRON or Samsung
◆ PROGRAM CLOCK	: Supported
◆ Maximum Speed	: 2400Mbps

10、FPGA原型验证平台：UV-19P-Q平台支持PCIE Gen3X8，提供PCIE功能卡。

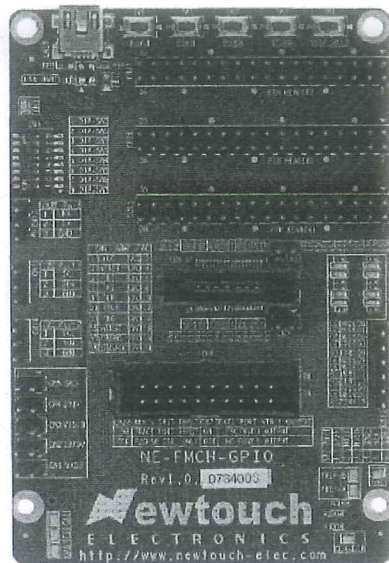
佐证材料：UVAPS-PM-011-00053-0A_2211 P14

- 8 HGC connectors to provide 32 GTY transceivers in total
- Supports high-speed interconnections and time division multiplexing between XCVU19Ps.
- Connects to the host computer through a PCIe Gen3 ×8 port.
- Supports remote power control of the XCVU19Ps through the runtime software UV APS Run.
- Supports remotely powering on/off the UV APS over Ethernet through the provided power module.
- Supports auto-partitioning by using the compilation tool UV APS Compiler.
- Provides a deep-tracing probing module to work with DDR4 daughter cards to capture a broad range of signals over a long time scale at fast speed.

11、FPGA原型验证平台：UV-19P-Q平台支持GPIO, URAT, I2C, 拨码开关, LED, ARM JTAG, 提供相关功能卡, 接口形式FMC。

佐证材料：详见网页

<http://www.phinedesign.cn/details.aspx?id=168>



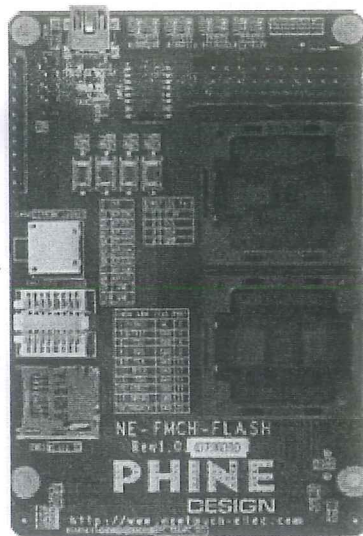
特性

- 提供ARM JTAG, Mictor-38接口
- 排针, UART, I2C, SPI接口
- 提供按钮, 双向拨码开关, LED灯等测试设备

12、FPGA原型验证平台: UV-19P-Q平台支持SDCard, NOR Flash, NAND Flash, EEPROM, 提供相关功能卡, 接口形式FMC。

佐证材料: 详见网页

<http://www.phinedesign.cn/details.aspx?id=152>



特性

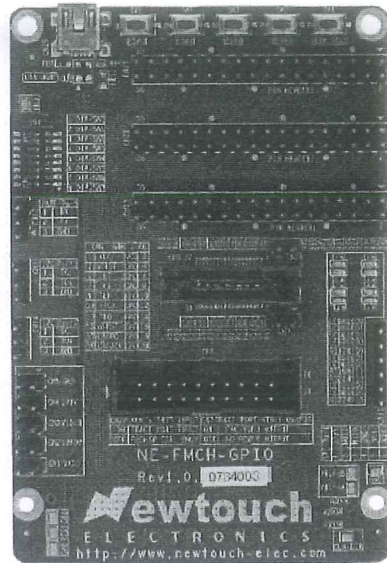
- 支持eMMC, SPI, Nor Flash, I2C, SD card, UART, USB-UART
- 按钮, 双向拨码开关
- ARM JTA

13、FPGA原型验证平台:UV-19P-Q平台支持CAN2.0提供相关功能卡,接口形式FMC。

佐证材料: 详见网页

通过 GPIO 的板卡可以实现该功能。

<http://www.phinedesign.cn/details.aspx?id=168>



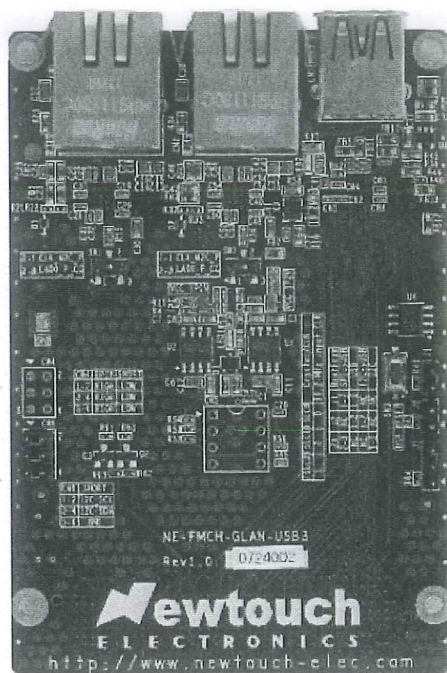
特性

- 提供ARM JTAG, Mictor-38接口
- 排针, UART, I2C, SPI接口
- 提供按钮, 双向拨码开关, LED灯等测试设备

14、FPGA原型验证平台: UV-19P-Q平台支持USB2.0与USB3.0, 提供相关功能卡, 接口形式FMC。

佐证材料: 详见网页

<http://www.newtouch-elec.com/details.aspx?id=154>



特性

- CYUSB3014(CYPRESS)
- 1000BASE-T PH(Marvell): 88E1111-B2-BAB1C000

15、FPGA原型验证平台：UV-19P-Q平台支持远程控制，上电断电。

佐证材料：UVAPS-PM-011-00053-0A_2211 P14

- 24 APC connectors to provide 1224 high performance IOs in total
- 8 HGC connectors to provide 32 GTY transceivers in total
- Supports high-speed interconnections and time division multiplexing between XCVU19Ps.
- Connects to the host computer through a PCIe Gen3 ×8 port.
- Supports remote power control of the XCVU19Ps through the runtime software UV APS Run.
- Supports remotely powering on/off the UV APS over Ethernet through the provided power module.
- Supports auto-partitioning by using the compilation tool UV APS Compiler.

16、FPGA原型验证平台：UV-19P-Q平台支持系统状态监测，过流过压保护，温度监测。

佐证材料：UV APS数据手册 P2

系统安全

- 系统状态/温度监测
- 过压/过流保护

17、FPGA原型验证平台：UV-19P-Q平台支持平台功能自检。

佐证材料：UVAPS-PM-011-00053-0A_2211 P36

4.3 Commissioning of the UV APS

This section describes the procedures to test different connections at the UV APS, including the connectors and fitted daughter cards.

About this task

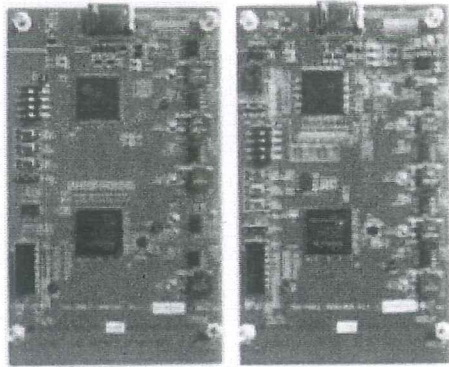
After installation of the UV APS or a daughter card, run the diagnostic scripts on the runtime software UV APS Run to examine:

- Connections at connectors
- Temperature, voltage, and the fan speed of each XCVU19P
- Working status of each XCVU19P

18、FPGA原型验证平台：UV-19P-Q平台支持HDMI功能，支持4K/2k 30Hz，提供HDMI功能卡，接口形式FMC。

佐证材料：详见网页

<http://www.phinedesign.cn/details.aspx?id=173>



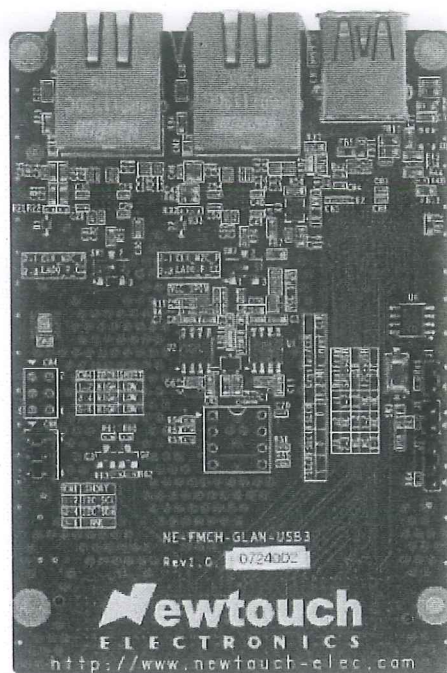
特性

- HDMI1.4 子卡, 支持 HDMI4K2K 30Hz 输入 / 输出

19、APS平台支持千兆网口, 提供功能卡, 接口形式FMC。

佐证材料: 详见网页

<http://www.newtouch-elec.com/details.aspx?id=154>



特性

- CYUSB3014(CYPRESS)
- 1000BASE-T PH(Marvell): 88E1111-B2-BAB1C000

20、FPGA原型验证平台：UV-19P-Q平台支持多平台级联应用。

佐证材料：UVAPS-PM-011-00053-0A_2211 P25

3.2 Control module

The control module sits on a dedicated FPGA to support communications between the host and the XCVU19Ps.

The control module serves:

- Communication with the host through the PCIe Gen3 ×8 port on the front panel.
- Access and configuration of the XCVU19Ps, including power, clock, and different interfaces shown in *Section 2.1, Block diagram*.
- Monitoring the temperature of each XCVU19P.
- Controlling the cooling fans.
- Connections between control boards of the cascaded UV APSes through connecting the B2B<n> connectors on the front panel.

21、FPGA原型验证平台：UV-19P-Q平台支持与PC主机进行数据交互。

佐证材料：

UVAPS-PM-011-00053-0A_2211 P2-4 P15

2.3 Interface connectors

Figure 2-2 shows the UV APS case, which is a 3U rackmount case to carry four Xilinx® Virtex® UltraScale+™ XCVU19P FPGAs (XCVU19Ps).

On the case surface, various different connectors make connections to peripheral devices and between XCVU19Ps easy.

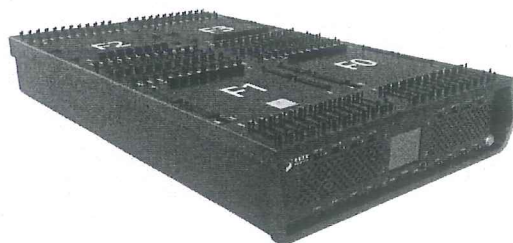


Figure 2-2 UV APS rackmount case

22：FPGA原型验证平台：UV-19P-Q平台支持FPGA信号的抓取和调试。

佐证材料：

UVAPS-PM-011-00053-0A_2211 P12 2-1

The UV APS is also equipped with runtime and signal probing software for easily controlling and debugging the FPGA signals at runtime to ease the verification process.

This chapter provides specifications of the UV APS. It contains the following sections:

23、FPGA原型验证平台：UV-19P-Q平台支持RTL逻辑综合，支持分布式并行模式，可以支持三态信号（tri-state）综合和跨模块信号参考（XMR）综合。

佐证材料：UVAPS-SW-UG-012-10054-0A_2211 P6-1 (P30)

Procedure

1. Elaborate the design with the following command:

```
elaborate <top_design_name>
```

2. Start synthesis with the following command:

```
synthesize_design
```

This command splits the design into different blocks and calls Xilinx® Vivado® to synthesize these blocks parallelly to gate-level netlists, which reduces much synthesis time.

These design blocks are saved to <workspace>/Synthesis/Rtl_elab/Src/<block_name>/.

The netlists of these blocks are saved to

<workspace>/Synthesis/Vivado/Edif/Src/<block_name>/.

3. When the synthesis completes, check the following reports:

- <execution_directory>/uvshell.log: The compiler runtime log file.
- <workspace>/Log/Elaboration.log: The elaboration summary log file.
- <workspace>/Log/Synthesis.log: The synthesis summary log file.
- <workspace>/Synthesis/Log/: This directory contains various synthesis result reports.

The frequently examined reports include:

- xmr_report.log: The crossing module reference handling report.
- strength_report.log: The multiple-driver and tri-state handling report
- init_val_report.log: The initial statement transforming report
- mem_report.log: The usage of different types of memory
- block_report.log: The report about the split design blocks and their synthesis details.

4. If the results are satisfactory, save the workspace with the following command:

```
save_working_space
```

5. (Optional) Exit the compiler by typing exit.

24、FPGA原型验证平台：UV-19P-Q平台支持门控时钟自动转换功能。

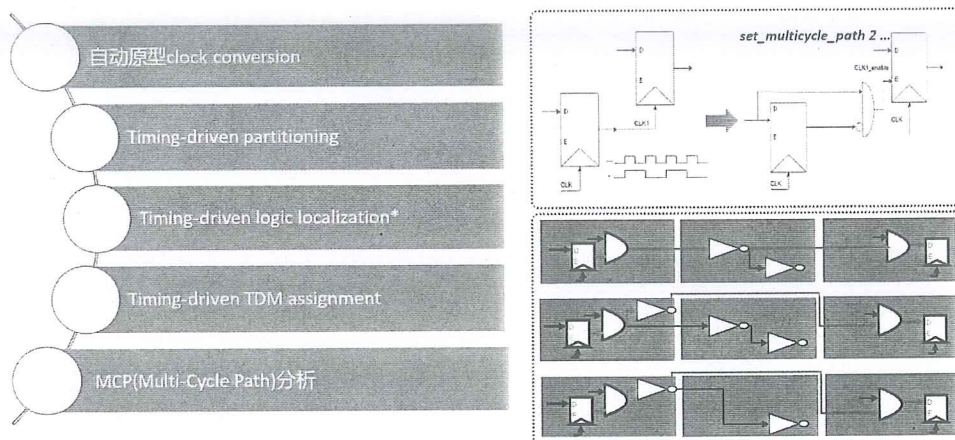
佐证材料：UVAPS-SW-UG-012-10054-0A_2211 P7-4 P35

The following figures show the reports generated in clock transformation.

- During clock transforming, the following report lists all the primary and gated clocks in the netlist. **OK** indicates the gated clock can be converted by the compiler.

Clock legal check summary:

Type	Result	Conn
Primary	AS IS	hnextclk
Primary	AS IS	io_pads_jtag_TCK_i_ival
Primary	AS IS	lnextclk
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_cpu_top/u_e203_cpu/u_e203_clk_ctrl/u_blu_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_cpu_top/u_e203_cpu/u_e203_clk_ctrl/u_dtcn_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_cpu_top/u_e203_cpu/u_e203_clk_ctrl/u_exu_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_cpu_top/u_e203_cpu/u_e203_clk_ctrl/u_ifu_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_cpu_top/u_e203_cpu/u_e203_clk_ctrl/u_itcn_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_cpu_top/u_e203_cpu/u_e203_clk_ctrl/u_lsu_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_cpu_top/u_e203_cpu/u_e203_dtcn_ctrl/u_sram_icb_ctrl/u_s1rv_1cyc_sram_ctrl/u_ram_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_cpu_top/u_e203_cpu/u_e203_itcn_ctrl/u_sram_icb_ctrl/u_s1rv_1cyc_sram_ctrl/u_ram_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_subsys_hclkgen/u_e203_subsys_gfcm/u_clk1_clkgate/HW KEEP_111_i_1/0
gater	OK	u_e203_subsys_top/u_e203_subsys_main/u_e203_subsys_hclkgen/u_e203_subsys_pllclkdiv/u_pllclkdiv_clkgate/HW KEEP_111_i_1/0



25、FPGA原型验证平台：UV-19P-Q平台支持16路可编程时钟网络。

佐证材料：

UVAPS-PM-011-00053-0A_2211 P14 P2-3

2.2 Features

Key features of the UV APS include:

- Per UV APS provides 4 Xilinx® Virtex® UltraScale+™ XCVU19P FPGAs (XCVU19Ps).
 - Per UV APS provides 20 programmable global clocks, 16 feedback clocks, and 4 resets.
These clocks and resets go through fanout buffers to produce four copies of clocks and resets.
Then, the four copies of clocks and resets feed the four XCVU19Ps respectively.
- For more details about the clocks, see *Section 3.3, Clock module*.

26、FPGA原型验证平台：UV-19P-Q平台支持多端口多维数组自动综合为片内或者片外存储资源。

佐证材料：UVAPS-SW-UG-012-10054-0A_2211 P28 P5-12

5.7 Mapping memory and black box modules

Use the following commands to map an array in the design to either the FPGA memory or an external memory daughter card, and identify the black box modules in the design:

- To map an **array** in the design memory to a memory component with the following command:

```
assign_memory -instance <instancePath> | -module <moduleName> -array_name <arrayName> \  
-type <memType> [-connector <fmcConnectorName>] [-lib <module_used_libName>]
```

In the above command line, -type supports the following memory types:

- **BRAM:** On FPGA
- **URAM:** On FPGA
- **LUTRAM:** On FPGA
- **EXSRAM:** On an external SRAM daughter card
When using this type, the card used FMC connector must be specified by
-connector b<i>F<j>_FMC<k>.
- **EXDDR:** On an external DDR daughter card
When using this type, the card used FMC connector must be specified by
-connector b<i>F<j>_FMC<k>.
- **FF:** bit-blast using flip-flops
- To identify the black box modules and the directories to their source IP information, type the following command:

```
set_blackbox -module <target_module> -directory <directory_to_blackbox_IP>
```

27、FPGA原型验证平台：UV-19P-Q平台支持向导分割模式和全自动分割模式。

佐证材料：UVAPS-PM-011-00053-0A_2211 P14 P2-3

5.2 (Optional) Setting manual partitions

You can configure a manual partition with the `create_group`, `create_partition`, and `create_fpga` commands. This section uses an example to demonstrate the use of these commands.

The `create_group` and `create_fpga` commands also support partitioning a block of a design onto multiple FPGAs. For details see *Section 5.2.1, Setting partitioning of a block to multiple FPGAs*.

For performing a partition, see *Chapter 8, Partitioning the design*.

About this task

Add the following settings to the partition constraint file if you prefer a manual partition to an auto-partition by the UV APS Compiler.

Procedure

1. Open the constraint Tcl file that you set for [mapping pins](#).
2. (Optional) Consult with the UniVista support engineer to change the default utilization rates of the FPGA resources by using the following command:

```
set_fill_rate -lut 50 -lut6 50 -ramlut 50 -reg 50 -carry8 50 -bram 50 -uram 50 -dsp 50
```

Where, 50 is the default value to represent 50%. Ideally, you can use any integer in (0,100).

To configure the resources on individual FPGAs, add the `-fpga b<i>.<j>.<k>` option.

3. Configure the manual partition as shown in the following example.

The figure below illustrates a partitioning example on a UV APS prototyping system:

- The left part shows the design contains the top and sub-module instances.
- The right part shows the expected partitioning results:
 - The top module instance, named **top**, goes to FPGA F0,
 - The submodule instance named **A** goes to FPGA F1.
 - The submodule instance named **B** and this submodules goes to FPGA F2.
 - The submodule instance named **E** and this submodules goes to FPGA F3

UVAPS-SW-UG-012-10054-0A_2211 P5-4 P20

- Supports high-speed interconnections and time division multiplexing between XCVU19Ps.
- Connects to the host computer through a PCIe Gen3 ×8 port.
- Supports remote power control of the XCVU19Ps through the runtime software UV APS Run.
- Supports remotely powering on/off the UV APS over Ethernet through the provided power module.
- Supports auto-partitioning by using the compilation tool UV APS Compiler.
- Provides a deep-tracing probing module to work with DDR4 daughter cards to capture a broad range of signals over a long time scale at fast speed.
- Controlled, monitored, and signal probed at runtime by the runtime software UV APS Run and the

28、FPGA原型验证平台：UV-19P-Q平台支持自动插入时分复用IP。

佐证材料：

UVAPS-PM-011-00053-0A_2211 P12 P2-1

2 Product overview

The UniVista Advanced Prototyping System (UV APS) is a large FPGA prototyping system to support high-performance and accurate ASIC and SoC verifications. It provides four connected Xilinx® Virtex® UltraScale+™ XCVU19Ps in one system, the Xilinx highest capacity FPGAs, and provides rich sets of connectors to easily assemble a large verification platform with various peripheral devices connected.

The UV APS is equipped with a robust and intelligent compiler engine, the UV APS Compiler, which automatically partitions and routes designs into the UV APS assisted by the time division multiplexing (TDM) IP to overcome shortage of I/O pins in FPGAs. With the UV APS Compiler, the time and difficulties in partitioning the design across FPGAs are dramatically reduced.

The UV APS is also equipped with runtime and signal probing software for easily controlling and debugging the FPGA signals at runtime to ease the verification process.

UVAPS-SW-UG-012-10054-0A_2211 P9 P1-1

1 Introduction

This book outlines the procedures to perform FPGA validations on the UniVista Advanced Prototyping System (UV APS) with the provided UV APS Toolkit.

The toolkit contains the following tools to perform synthesis, automatic partitioning, placement and routing (PnR) across FPGAs, and runtime control to waveform debugging:

- **UV APS Compiler:** A timing driven multi-FPGA partitioning and high efficient compiler to cover synthesis, partitioning, time division multiplexing (TDM) and other IP insertions, and PnR all in one.
- **UV APS Run:** A multifunctional runtime command line tool to control the UV APS, read status, and capture a large number of signals to probe in real time.
- **UniVista Debugger (UVD):** An intuitive GUI debugging tool to debug the captured USDB waveforms in a more interactive, precise, and faster way.

Note: USDB is short for UniVista Signal Data Base, which is a UniVista proprietary waveform format to provide a smaller size but more debugging utilities than the VCD.

This chapter contains the following sections:

29、FPGA原型验证平台：UV-19P-Q平台支持将设计中大规模存储映射到子卡的功能。

佐证材料：

UVAPS-SW-UG-012-10054-0A_2211 P21 P5-12

5.7 Mapping memory and black box modules

Use the following commands to map an array in the design to either the FPGA memory or an external memory daughter card, and identify the black box modules in the design:

- To map an array in the design memory to a memory component with the following command:

```
assign_memory -instance <instancePath> | -module <moduleName> -array_name <arrayName> \  
-type <memType> [-connector <fmcConnectorName>] [-lib <module_used_libName>]
```

In the above command line, -type supports the following memory types:

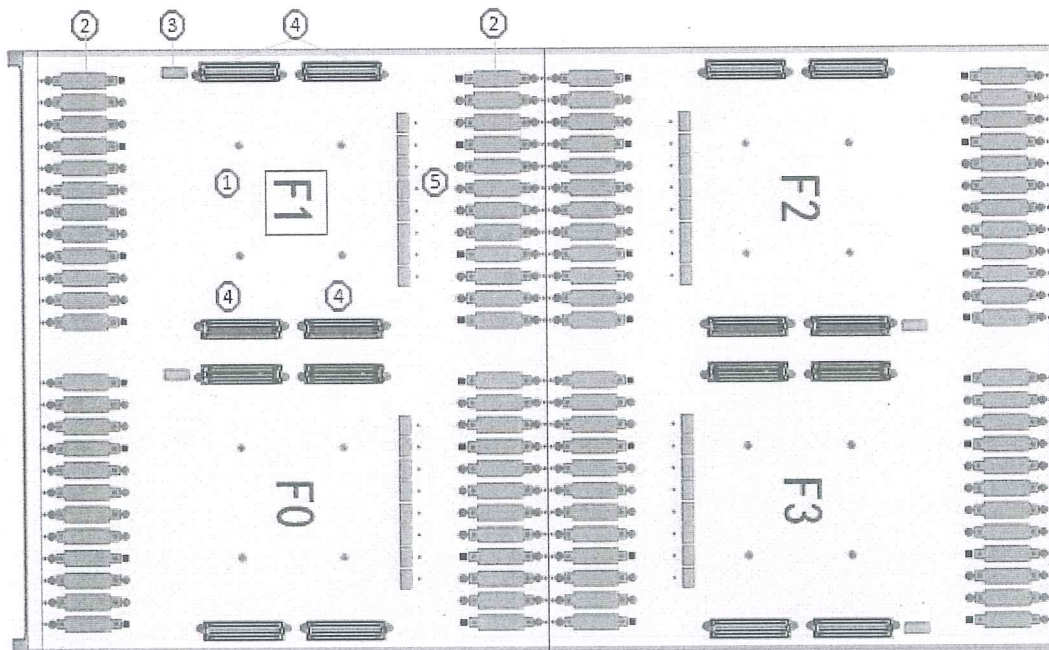
 - BRAM:** On FPGA
 - URAM:** On FPGA
 - LUTRAM:** On FPGA
 - EXSRAM:** On an external SRAM daughter card
When using this type, the card used FMC connector must be specified by
-connector b<i>F<j>_FMC<k>.
 - EXDDR:** On an external DDR daughter card
When using this type, the card used FMC connector must be specified by
-connector b<i>F<j>_FMC<k>.
 - FF:** bit-blast using flip-flops
- To identify the black box modules and the directories to their source IP information, type the following command:

```
set_blackbox -module <target_module> -directory <directory_to_blackbox_IP>
```

30、FPGA原型验证平台：UV-19P-Q平台支持通过FMC接口扩展板卡功能。

佐证材料：

UVAPS-PM-011-00053-0A_2211 P18 P2-7



31、FPGA原型验证平台：UV-19P-Q平台支持基于RISC-V的原型验证功能。

佐证材料：

32、FPGA原型验证平台：UV-19P-Q平台支持PCIE，以太网，USB高速通信协议。

佐证材料：Product Manual Daughter Cards

 丰富的子卡资源	
General Purpose	通用排针子卡
	通用接口调试子卡
	FMC转QTH子卡
	loopback测试卡
	SRAY3转换卡
	FMC转One bank connector
	FMC转HOB子卡
High Speed	千兆网口/USB3.0子卡
	USB3PHY
	SAS转PCIE Endpoint子卡 (Gen3x8)
	PCIE Endpoint子卡 (Gen3x8)
	SAS转接卡
	PCIE Root子卡 (Gen3x8)
	SAS接口 100G光口子卡
	FMC 100G光口子卡
Memory	ETH-Nor flash-Nand-USB2.0
	低速存储接口子卡
	SRAM子卡
	DDR4 SODIMM ECC for VU plus prototyping platform
	DDR3 SODIMM ECC for VU plus prototyping platform
	DDR4 for VU plus prototyping platform
	Memory Adapter
	NAND Flash子卡
Video & Broadcast	LVDs子卡
	*12G-SDI广播子卡
	*Display port子卡 (1.4spec)
	HDMI4K 30子卡
	*V-by-one子卡
	MIPI CSI子卡
	*HDMI4K 60子卡

33、FPGA原型验证平台：UV-19P-Q平台支持支持FPGA之间通过TDM IP互联。

佐证材料：

UVAPS-PM-011-00053-0A_2211 P12 P2-1

2 Product overview

The UniVista Advanced Prototyping System (UV APS) is a large FPGA prototyping system to support high-performance and accurate ASIC and SoC verifications. It provides four connected Xilinx® Virtex® UltraScale+™ XCVU19Ps in one system, the Xilinx highest capacity FPGAs, and provides rich sets of connectors to easily assemble a large verification platform with various peripheral devices connected.

The UV APS is equipped with a robust and intelligent compiler engine, the UV APS Compiler, which automatically partitions and routes designs into the UV APS assisted by the time division multiplexing (TDM) IP to overcome shortage of I/O pins in FPGAs. With the UV APS Compiler, the time and difficulties in partitioning the design across FPGAs are dramatically reduced.

The UV APS is also equipped with runtime and signal probing software for easily controlling and debugging the FPGA signals at runtime to ease the verification process.

34、FPGA原型验证平台：UV-19P-Q平台支持自动识别XMR功能。

佐证材料：

UVAPS-SW-UG-012-10054-0A_2211 P6-1 (P30)

Procedure

1. Elaborate the design with the following command:

```
elaborate <top_design_name>
```

2. Start synthesis with the following command:

```
synthesize_design
```

This command splits the design into different blocks and calls Xilinx® Vivado® to synthesize these blocks parallelly to gate-level netlists, which reduces much synthesis time.

These design blocks are saved to <workspace>/Synthesis/Rtl_elab/Src/<block_name>/.

The netlists of these blocks are saved to

```
<workspace>/Synthesis/Vivado/Edif/Src/<block_name>/.
```

3. When the synthesis completes, check the following reports:

- <execution_directory>/uvshell.log: The compiler runtime log file.
- <workspace>/Log/Elaboration.log: The elaboration summary log file.
- <workspace>/Log/Synthesis.log: The synthesis summary log file.
- <workspace>/Synthesis/Log/: This directory contains various synthesis result reports.

The frequently examined reports include:

- xmr_report.log: The crossing module reference handling report.
- strength_report.log: The multiple-driver and tri-state handling report
- init_val_report.log: The initial statement transforming report
- mem_report.log: The usage of different types of memory
- block_report.log: The report about the split design blocks and their synthesis details.

4. If the results are satisfactory, save the workspace with the following command:

```
save_working_space
```

5. (Optional) Exit the compiler by typing exit.

35、FPGA原型验证平台：UV-19P-Q平台支持软件复位功能。

佐证材料：

UVAPS-SW-UG-012-10054-0A_2211 P13-4 (P49)

7. Configure the reset signals as follows:

- a. Query the reset signals from the database with the following command:

```
query -reset
```

This command shows the resets as follows, where the last column shows the reset name:

```
apxrun> query -reset
query -reset
```

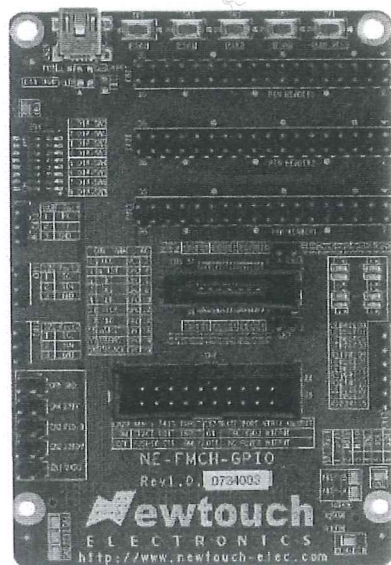
Board	Index	Polarity	Reset Name
B0	0	1	rst

Note: For the UV APS prototyping system, up to 4 resets are provided.

- b. Assert resets one by one with the following command:

36、FPGA 原型验证平台：UV-19P-Q 平台支持 FPGA 逻辑代码的比特流下载与校验。

佐证材料：



特性

- 提供ARM JTAG, Mictor-38接口
- 排针, UART, I2C, SPI接口
- 提供按钮, 双向拨码开关, LED灯等测试设备

<https://docs.xilinx.com/v/u/en-US/ds593>

Features

- High-performance FPGA and PROM programming and configuration
 - Includes innovative FPGA-based acceleration firmware encapsulated in a small form factor pod attached to the cable
 - Leverages high-speed slave-serial mode programming interface
 - Note:** Slave-serial mode is supported in Xilinx® iMPACT software v10.1.
 - Recommended for prototyping use only
- Easy to use
 - Fully integrated and optimized for use with Xilinx iMPACT software
 - Intuitive multiple cable management from a single application
 - Supported on the following operating systems:
 - Note:** See the Xilinx design tool release notes for supported operating systems.
 - Microsoft Windows XP Professional
 - Microsoft Windows Vista
 - Red Hat Enterprise Linux
 - SUSE Linux Enterprise
 - Automatically senses and adapts to target I/O voltage
 - Interfaces to devices operating at 5V (TTL), 3.3V (LVCMOS), 2.5V, 1.8V and 1.5V
 - Intuitive flyleads-to-cable interface labeling
- Reliable
 - Backwards compatibility with Platform Cable USB, including Pb-Free (RoHS-compliant)
 - USB Integrators Forum (USB-IF) certified
 - CE and FCC compliant
 - Leverages industry standards, including JTAG boundary-scan IEEE 1149.1, SPI and USB 2.0
- Programs and configures all Xilinx devices
 - XC18V00 ISP PROMs
 - Platform Flash XCF00S/XCF00P/XL PROMs
 - All UltraScale™, 7 series, Virtex®, and Spartan® FPGA families, and Zynq-7000 SoCs
 - XC9500XL and CoolRunner™ XPLA3 / CoolRunner-II CPLDs
 - Note:** Xilinx iMPACT software or Vivado design tools are required for programming and configuration. See the design tool release notes for supported devices.
- Third-party PROM device programming support
 - Directly programs selected Serial Peripheral Interface (SPI) flash memory devices
 - Note:** Direct SPI flash memory programming supported in Xilinx iMPACT software v10.1.
 - Indirectly programs selected SPI or parallel flash memory devices via FPGA JTAG port
- Highly optimized for use with Xilinx design tools
 - Vivado® design tools or ISE® design tools
 - Embedded Development Kit
 - ChipScope™ Pro Analyzer
 - System Generator for DSP

Platform Cable USB II Description

Much more than just a simple USB cable, Platform Cable USB II (Figure 1) provides integrated firmware (hardware and software) to deliver high-performance, reliable and easy-to-perform configuration of Xilinx devices.

Platform Cable USB II attaches to user hardware for the purpose of configuring Xilinx FPGAs, programming Xilinx

PROMs and CPLDs, and directly programming third-party SPI flash devices. In addition, the cable provides a means of indirectly programming Platform Flash XL, third-party SPI flash memory devices, and third-party parallel NOR flash memory devices via the FPGA JTAG port. Furthermore, Platform Cable USB II is a cost effective tool for debugging

37、FPGA 原型验证平台：UV-19P-Q 平台支持基于 Xilinx 芯片的 FPGA 集成开发平台，可实现 FPGA 开发、编译、调试、烧写功能。

佐证材料：

Table 2-5 lists the software and operating system (OS) used with the UV APS.

Table 2-5 Software used with the UV APS

Item	Description
Compiler	UV APS Compiler, version 2022.10
Runtime	UV APS Run, version 2022.10
UniVista Debugger	UVD, version 2022.06.P3
OS	CentOS 7.8
Synthesis, placement, and routing	Xilinx® Vivado®, version 2021.2



Platform Cable USB II

DS593 (v1.5.1) August 6, 2018

Features

- High-performance FPGA and PROM programming and configuration
 - Includes innovative FPGA-based acceleration firmware encapsulated in a small form factor pod attached to the cable
 - Leverages high-speed slave-serial mode programming interface

Note: Slave-serial mode is supported in Xilinx® iMPACT software v10.1.
 - Recommended for prototyping use only
- Easy to use
 - Fully integrated and optimized for use with Xilinx iMPACT software
 - Intuitive multiple cable management from a single application
 - Supported on the following operating systems:

Note: See the Xilinx design tool release notes for supported operating systems.

 - Microsoft Windows XP Professional
 - Microsoft Windows Vista
 - Red Hat Enterprise Linux
 - SUSE Linux Enterprise
 - Automatically senses and adapts to target I/O voltage
 - Interfaces to devices operating at 5V (TTL), 3.3V (LVCMOS), 2.5V, 1.8V and 1.5V
 - Intuitive flyleads-to-cable interface labeling
- Reliable
 - Backwards compatibility with Platform Cable USB, including Pb-Free (RoHS-compliant)
 - USB Integrators Forum (USB-IF) certified
 - CE and FCC compliant
 - Leverages industry standards, including JTAG boundary-scan IEEE 1149.1, SPI and USB 2.0
- Programs and configures all Xilinx devices
 - XC18V00 ISP PROMs
 - Platform Flash XCF00S/XCF00P/XL PROMs
 - All UltraScale™, 7 series, Virtex®, and Spartan® FPGA families, and Zynq-7000 SoCs
 - XC9500XL and CoolRunner™ XPLA3 / CoolRunner-II CPLDs

Note: Xilinx iMPACT software or Vivado design tools are required for programming and configuration. See the design tool release notes for supported devices.
- Third-party PROM device programming support
 - Directly programs selected Serial Peripheral Interface (SPI) flash memory devices

Note: Direct SPI flash memory programming supported in Xilinx iMPACT software v10.1.
 - Indirectly programs selected SPI or parallel flash memory devices via FPGA JTAG port
- Highly optimized for use with Xilinx design tools
 - Vivado® design tools or ISE® design tools
 - Embedded Development Kit
 - ChipScope™ Pro Analyzer
 - System Generator for DSP

Platform Cable USB II Description

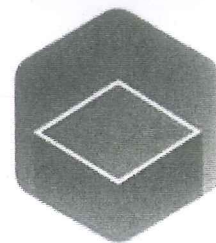
Much more than just a simple USB cable, Platform Cable USB II (Figure 1) provides integrated firmware (hardware and software) to deliver high-performance, reliable and easy-to-perform configuration of Xilinx devices.

Platform Cable USB II attaches to user hardware for the purpose of configuring Xilinx FPGAs, programming Xilinx

PROMs and CPLDs, and directly programming third-party SPI flash devices. In addition, the cable provides a means of indirectly programming Platform Flash XL, third-party SPI flash memory devices, and third-party parallel NOR flash memory devices via the FPGA JTAG port. Furthermore, Platform Cable USB II is a cost effective tool for debugging

38、FPGA原型验证平台：UV-19P-Q平台该数据包包括开源处理器相关部分的rtl代码和在APS可以运行的database。系统包括了SD和DDR外设。此设计放到4片FPGA后，同时linux可以正常引导到命令行阶段。

佐证材料：详见openpiton定制化脚本源码、synbck_man、sim_man、micro_arch、fpga_man、carrv2019_paper_12。



合见工软

UniVista

Advanced Prototyping System

Product Manual

Rev. 0A, Nov. 2022

Confidential

Copyright © 2022 UniVista. All rights reserved.

Doc No. 011-00053

Legal notices

Copyright Information

This document is protected by copyright and other related rights. The practice or implementation of the information contained in this document may be protected by one or more patents or pending patent applications. No part of this document may be reproduced in any form by any means without the express prior written permission of UniVista.

The information in this manual is subject to change without notice and should not be construed as a commitment by UniVista. This document may include technical inaccuracies or typographical errors. UniVista assumes no responsibility for any errors that may appear in this manual.

THIS DOCUMENT IS PROVIDED "AS IS". UNIVISTA PROVIDES NO REPRESENTATIONS AND NO WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, SATISFACTORY QUALITY, NON-INFRINGEMENT OR FITNESS FOR A PARTICULAR PURPOSE WITH RESPECT TO THE DOCUMENT.

IN NO EVENT WILL UNIVISTA BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT AND PRODUCTS DESCRIBED HEREIN, EVEN IF UNIVISTA HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Deliverables-Property of Shanghai UniVista Industrial Software Group Co., Ltd.

This deliverable is confidential and proprietary information of Shanghai UniVista Industrial Software Group Co., Ltd. This deliverable shall not be copied, modified, re-published, uploaded, executed, distributed, transmitted or translated in any way, in any medium, whether in whole or in part, without the prior written consent of Shanghai UniVista Industrial Software Group Co., Ltd. or as expressly provided by the license agreement.

This deliverable is for the sole purpose of information and instruction. Shanghai UniVista Industrial Software Group Co., Ltd. reserves the right to make changes in this deliverable at its own discretion without any prior notice.

Disclaimer of Warranty

SHANGHAI UNIVISTA INDUSTRIAL SOFTWARE GROUP CO., LTD. AND ITS LICENSOR MAKE NO REPRESENTATIONS OR WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY,

FITNESS FOR A PARTICULAR PURPOSE, TITLE OR NON-INFRINGEMENT, AND ALL WARRANTIES THAT MAY ARISE FROM COURSE OF PERFORMANCE, COURSE OF DEALING OR USAGE OF THIS DELIVERABLE. IN NO EVENT WILL SHANGHAI UNIVISTA INDUSTRIAL SOFTWARE GROUP CO., LTD. AND ITS LICENSOR BE LIABLE FOR ANY LOSS OF PROFITS, LOSS OF BUSINESS, LOSS OF USE OR DATA, INTERRUPTION OF BUSINESS, OR FOR ANY INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES OF ANY KIND, EVEN IF SHANGHAI UNIVISTA INDUSTRIAL SOFTWARE GROUP CO., LTD. HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Trademarks

The trademarks and logos ("Trademark") used herein are the trademarks of Shanghai UniVista Industrial Software Group Co., Ltd. or a third party. No one is authorized to use such Trademark without the prior written consent of Shanghai UniVista Industrial Software Group Co., Ltd. or the owner of such Trademark, as applicable. The use of Trademark of a third party herein is intended solely to indicate a product from, or associated with, a particular third party.

Copyright © 2022 Shanghai UniVista Industrial Software Group Co., Ltd. All rights reserved worldwide.

Contents

Legal notices.....	i
Contents	iii
Change history.....	iv
Preface	v
About this book	v
Intended audience.....	v
References.....	v
Conventions	vi
Glossary	vii
1 Safety	1-1
1.1 Electrostatic discharge precautions	1-2
1.2 Safety precautions.....	1-3
2 Product overview.....	2-1
2.1 Block diagram.....	2-2
2.2 Features	2-3
2.3 Interface connectors.....	2-4
2.3.1 Front view.....	2-5
2.3.2 Top view	2-7
2.3.3 Rear view	2-9
2.4 Technical data	2-10
2.5 System software.....	2-11
3 Module description	3-1
3.1 Power LEDs	3-2
3.2 Control module.....	3-3
3.3 Clock module.....	3-4
3.4 B2B cascading interface	3-6
3.5 Signal probing module	3-7
4 Installation, commissioning, and maintenance	4-1
4.1 Delivery list.....	4-2
4.2 Installing the UV APS	4-4
4.3 Commissioning of the UV APS.....	4-6
4.4 Troubleshooting.....	4-7
5 Performing prototyping.....	5-1
5.1 Prototyping workflow on the UV APS.....	5-2
A Appendix A: UV APS drawings.....	A-1
B Appendix B: FMC pin list	B-1

Change history

The following table lists the changes between document revisions.

Revision	Product revision ¹	Description
0A	1.0	Initial release.

1. SW products use *Product version*. HW products use *Product revision*.

Preface

This preface introduces the *UniVista Advanced Prototyping System Product Manual*.

About this book

This book describes the features and components of the UniVista Advanced Prototyping System (UV APS). It also outlines the procedures in installation and operation.

Intended audience

Readers of this book shall be system administrators, verification engineers, AEs, service engineers, or readers who are interested in the UV APS.

References

The following articles contain the information relevant to this book:

- *UV APS Software User Guide, 005-10005*
- *Xilinx® UltraScale® Architecture and Product Data Sheet: Overview, DS890*
- https://fmchub.github.io/appendix/VITA57_FMC_HPC_LPC_SIGNALS_AND_PINOUT.html






Conventions

Conventions include graphics, typographical conventions, and safety symbols used in this book.

- Graphics and screenshots contained in this book are for demonstration use only. They may vary from the product version you use.
- The following table describes the typographical conventions used in this book.

Style	Description
<code><placeholder></code>	In file paths, directories, and command lines, replaceable items use italics surrounded with <code><></code> .
<code>[option]</code>	In a command line, optional items are surrounded with <code>[]</code> .
<code>a b c</code>	In a command line, one of the provided choices must be selected
<code><u>option</u></code>	For a command-line option, the underlined part is an alternate of this option. Example: <code><u>-h</u>elp</code> means typing <code>-h</code> or <code>-help</code> are equivalent.
<code>\</code>	In a command line, the trailing <code>\</code> denotes a line continuation.
<code>...</code>	In a command line, <code>...</code> denotes repetitions of the preceding item.

- The following table describes the safety symbols used in the book. The keywords of the symbols denote different hazard levels of dangerous situations where personal injury is possible.

Safe symbol	Description
 DANGER!	Indicates a hazardous situation which, if not avoided, will result in death or serious or irreversible personal injury.
 WARNING!	Indicates a hazardous situation which, if not avoided, could result in death or serious or irreversible personal injury.
 CAUTION!	Indicates a hazardous situation which, if not avoided, may result in minor or moderate personal Injury.
 IMPORTANT!	Provides important information related to the content.
 ESD!	Electrostatic discharge (ESD) Warns for electrostatic hazards which could result in severe damage to the product.

Glossary

This glossary explains terms, acronyms, and abbreviations used in this book:

- **CLI:** Command Line Interface
- **FMC:** FPGA Mezzanine Card connectors on the UV APS
- **HGC:** Hundred Giga Connectors on the UV APS to provide GTY transceivers
- **APC:** Advanced Prototyping Connectors on the UV APS to provide high-performance IOs
- **HPC:** High Pin Count
- **PCIe:** Peripheral Component Interconnect Express
- **USDB:** Unified Signal Database

A waveform database developed by UniVista to provide a more compact waveform format but with more debugging capabilities than the VCD format.

- **Crosspoint switch:** A crosspoint switch directs signals of multiple inputs to any output.

1 Safety

Carefully read through the safety instructions listed in this chapter before or during your installation, operation, adjustment, or maintenance of the UniVista Advanced Prototyping System (UV APS). Failure to comply with the safety instructions can result in personal injury or property damages.

**IMPORTANT!**

Any safety information given in this manual must not be construed as a warranty by UniVista that the UV APS will not cause injury or damage even if all safety instructions are fully complied with.

This chapter contains the following sections:

- 1.1 *Electrostatic discharge precautions*
- 1.2 *Safety precautions*

1.1 Electrostatic discharge precautions

Electrostatic discharge (ESD) is the transfer of electrical static charge between two bodies at different potentials, either through direct contact or through an induced electrical field. When handling parts or their containers, personnel not grounded may potentially transfer high static charges. This discharge may destroy sensitive electronics.



ESD!

The UV APS is sensitive to electrostatic discharge (ESD), which may damage sensitive electronic components of the UV APS. Make sure to handle the system and plug-in components in an ESD secured environment.

The following instructions must be carefully followed:

- Ensure the UV APS is transported in static preventive material.
- Always wear a properly grounded wrist strap when physically contacting with the UV APS system, including touching the equipment shelves, handling, removing, or inserting cables, daughter cards, or power supply.
- Provide an ESD secured environment for installing and operating the UV APS, including using ESD protective flooring, such as an ESD protective floor mat or table mat, used with proper ESD footwear.
- Test the ESD wrist straps and footwear daily to ensure they operate correctly.

1.2 Safety precautions

Before you install, use, or service the UV APS, do read the following safety precautions first:

- Only qualified technicians can install, operate, maintain, and service the UV APS.
- Never perform hot plugging.

Always power off the UV APS before performing any procedures that require physically contact with the UV APS system, including connection of cables, daughter cards, and power supply.
- Handle the system by the baseplate but not by the frame.
- Immediately power off the UV APS for any emergency, such as fire, electric shock, or unpleasant smell. And then report the incident to the UniVista support engineers.
- Do not disassemble, repair, or modify the UV APS by yourself.
- Never touch a cooling fan when it is rotating.
- Do not touch the gold-plated parts on the UV APS.

Otherwise, the surface can contain sweat or skin oil, which can lead to contact failure, malfunction, electric shock, or fire from static electricity.
- Do not touch the UV APS with a metallic object, which may result in electric shock or fire.
- Keep the system dry and never touch it with a wet hand.
- If the UV APS is dropped or damaged, do not try to power on and use it.

Otherwise, electronic shock or fire may occur.
- Make sure the installation location is:
 - Firm and stable.
 - Clean and dry.
 - Well-ventilated to allow air flow for proper operation of the system.
 - Keep far away from direct sunlight, smoke, water, steam, chemicals, and heating systems.
- Do not place any object on the UV APS.

2 Product overview

The UniVista Advanced Prototyping System (UV APS) is a large FPGA prototyping system to support high-performance and accurate ASIC and SoC verifications. It provides four connected Xilinx® Virtex® UltraScale+™ XCVU19Ps in one system, the Xilinx highest capacity FPGAs, and provides rich sets of connectors to easily assemble a large verification platform with various peripheral devices connected.

The UV APS is equipped with a robust and intelligent compiler engine, the UV APS Compiler, which automatically partitions and routes designs into the UV APS assisted by the time division multiplexing (TDM) IP to overcome shortage of I/O pins in FPGAs. With the UV APS Compiler, the time and difficulties in partitioning the design across FPGAs are dramatically reduced.

The UV APS is also equipped with runtime and signal probing software for easily controlling and debugging the FPGA signals at runtime to ease the verification process.

This chapter provides specifications of the UV APS. It contains the following sections:

- *2.1 Block diagram*
- *2.2 Features*
- *2.3 Interface connectors*
- *2.4 Technical data*
- *2.5 System software*

2.1 Block diagram

Figure 2-1 shows the functional block diagram of the UV APS.

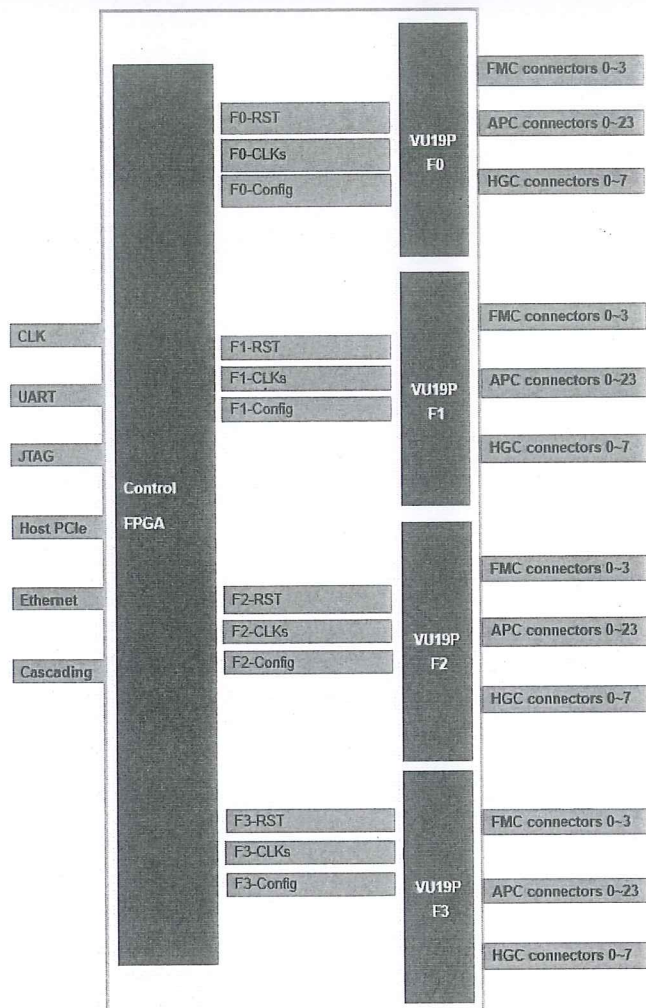


Figure 2-1 Functional block diagram of the UV APS

2.2 Features

Key features of the UV APS include:

- Per UV APS provides 4 Xilinx® Virtex® UltraScale+™ XCVU19P FPGAs (XCVU19Ps).
- Per UV APS provides 20 programmable global clocks, 16 feedback clocks, and 4 resets.
These clocks and resets go through fanout buffers to produce four copies of clocks and resets.
Then, the four copies of clocks and resets feed the four XCVU19Ps respectively.
For more details about the clocks, see *Section 3.3, Clock module*.
- Connectors on each XCVU19P include:
 - 4 high-pin count FMC connectors to provide 596 IOs and 14 GTY transceivers in total
Each FMC connector supports adjustable voltages from 1.0V to 1.8V.
 - 24 APC connectors to provide 1224 high performance IOs in total
 - 8 HGC connectors to provide 32 GTY transceivers in total
- Supports high-speed interconnections and time division multiplexing between XCVU19Ps.
- Connects to the host computer through a PCIe Gen3 ×8 port.
- Supports remote power control of the XCVU19Ps through the runtime software UV APS Run.
- Supports remotely powering on/off the UV APS over Ethernet through the provided power module.
- Supports auto-partitioning by using the compilation tool UV APS Compiler.
- Provides a deep-tracing probing module to work with DDR4 daughter cards to capture a broad range of signals over a long time scale at fast speed.
- Controlled, monitored, and signal probed at runtime by the runtime software UV APS Run and the waveform debugging tool UniVista Debugger (UVD).
- Full register visibility.
- Memory backdoor access to external DDRs, SRAMs, and flash memories.

2.3 Interface connectors

Figure 2-2 shows the UV APS case, which is a 3U rackmount case to carry four Xilinx® Virtex® UltraScale+™ XCVU19P FPGAs (XCVU19Ps).

On the case surface, various different connectors make connections to peripheral devices and between XCVU19Ps easy.

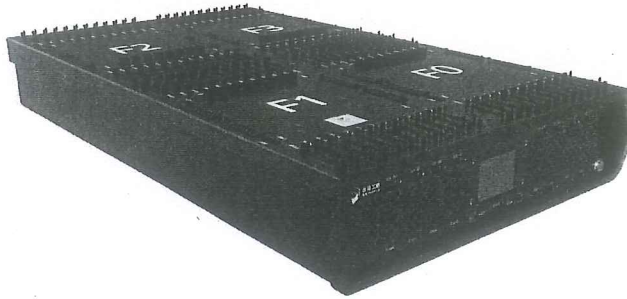


Figure 2-2 UV APS rackmount case

The following subsections describe the connectors at the front, top, and rear of the UV APS.

See also

2.4 Technical data

2.3.1 Front view

The following figure and table explain the components on the front panel of the UV APS.

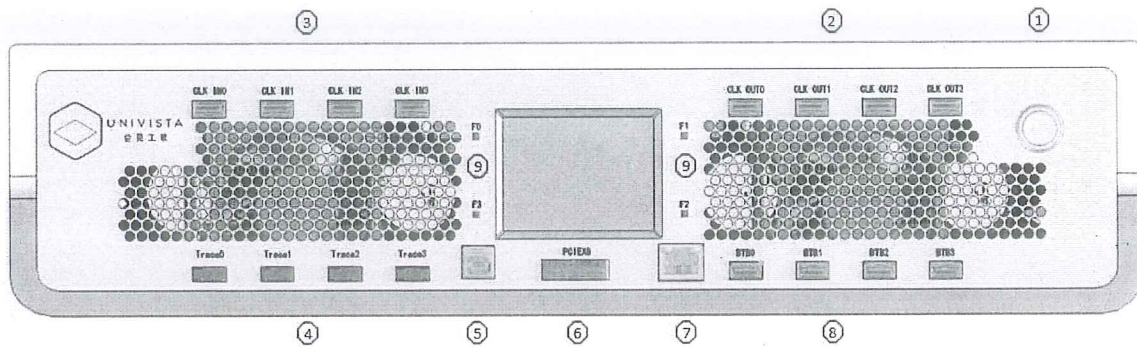


Figure 2-3 Front view of the UV APS

Table 2-1 Front panel components

Callout	Component name	Description	Connection cable
1	Power button	The power button of the UV APS.	-
2	CLK OUT0 to CLK OUT3	Used for master-slave connections to provide clocks and resets to the slave UV APSes. Each clock output port provides 5 clocks and 1 reset to the slave system at the counterpart clock input port of the slave. Note: In the current master-slave connections, the CLK OUT0 to CLK IN0 pair must be connected. For more details, see <i>Section 3.3, Clock module</i> .	-
3	CLK IN0 to CLK IN3	Used for master-slave connections to receive clocks and resets from the master UV APSes, as described in the row above. For clock specifications, see <i>Section 2.4, Technical data</i> .	-
4	Trace0 to Trace3	Reserved for future use. Each connector enables both a UART and a JTAG debugging of the associated XCVU19P by using a converter. On the converter, a UART-to-USB Type-C interface and an ARM JTAG 20 interface are provided.	-
5	USB	Reserved for future use.	-

Callout	Component name	Description	Connection cable
6	PCIEX8	Connects to the host computer through a PCIe Gen3 ×8 connection to transfer data between the host and UV APS rapidly and to enable a fast waveform debugging.	<ul style="list-style-type: none"> On the host, install a PCIe 8-lane daughter card UV-SASX8-PCIE. On the UV APS, connect the PICEX8 connector to the UV-SASX8-PCIE card through a cable, UV-IOC-<i><length_mm></i>.
7	ETH	An RJ-45 1G bps connector for system upgrade use only.	Standard Ethernet cable
8	B2B0 to B2B3	<p>Connect between the master and slave UV APSes.</p> <p>Currently, on the master any B2B<n> can be used. On the slave, B2B0 must be used.</p> <p>For more details, see <i>Section 3.4, B2B cascading interface</i>.</p>	-
9	Power LEDs	<p>The four LEDs indicate the power status of the four XCVU19Ps respectively.</p> <p>For more details, see <i>Section 3.2, Power status LEDs</i>.</p>	-

See also*4.1 Delivery list*

2.3.2 Top view

The following figure and table explain the components at the top of the UV APS. For a close view of the locations and indexes of the components, see *Appendix A: UV APS drawings*.

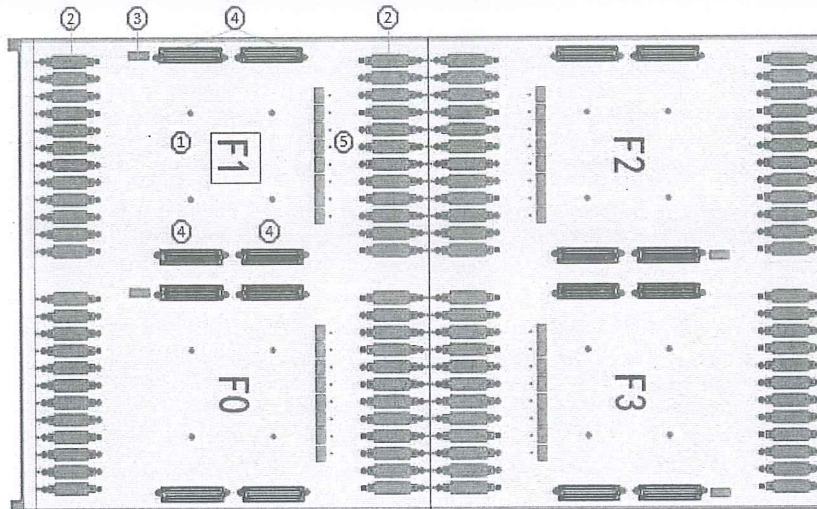


Figure 2-4 Top view of the UV APS

Table 2-2 Components at top

Callout	Component name	Description	Cable
1	F0 to F3	4 × XCVU19Ps	-
2	APC0 to APC23	<p>24 × APC connectors</p> <p>They provide high-performance IOs to interconnect between XCVU19Ps.</p> <p>Interconnections are done by converters UV-OBO-SAS, UV-OSM-SAS, and cables as follows:</p> <ul style="list-style-type: none"> APC0 to APC11 use interface converters UV-OBO-SAS. APC12 to APC23 use interface converters UV-OBM-SAS. Between the converters on different XCVU19Ps, connect them with the UV-IOC-<i><length_mm></i> cables. <p>Each APC connector:</p> <ul style="list-style-type: none"> Provides 51 IOs, including 24 differential pairs and 3 single-end signals. Supports up to 1.6 Gbps data rates per differential pair. Occupies 1 bank of the XCVU19P. 	<ul style="list-style-type: none"> Converters UV-OBO-SAS on APC0 to APC11. Converters UV-OBM-SAS on APC12 to APC23. cables UV-IOC-<i><length_mm></i>.

Callout	Component name	Description	Cable
2	HGC0 to HGC7	<p>8 × HGC connectors</p> <p>The 8 HGC connectors provide 32 GTY transceivers in total. They serve to interconnect between XCVU19Ps.</p> <p>Each HGC connector:</p> <ul style="list-style-type: none"> Provides 4 GTY transceivers to support 1 GTY quad of the XCVU19P. Supports up to 28.21 Gbps GTY line rate. 	<p>UV-HGC- <length_mm></p>
3	JTAG	2 mm JTAG header to support both programming and debugging the corresponding XCVU19P.	Xilinx JTAG download cables, such as the Xilinx® Platform Cable USB II.
4	FMC0 to FMC3	<p>4 × FMC connectors</p> <p>They are high-pin count (HPC) FMC connectors to connect to daughter cards or interconnect with XCVU19Ps.</p> <p>Each FMC connector:</p> <ul style="list-style-type: none"> Provides 149 IOs including 70 differential pairs and 9 single-end signals. Occupies 3 banks of the XCVU19P. Supports adjustable IO voltages from 1.0V to 1.8V. Supports interconnections with XCVU19Ps by using the daughter cards UV-FMCH-OBU1 and cables UV-IOC-<length_mm>. <p>FMC0 to FMC2 provide 14 GTY transceivers as follows:</p> <ul style="list-style-type: none"> FMC0: Provides 8 GTY transceivers to support PCIe ×8, PCIe ×4, and PCIe ×1. FMC1: Provides 4 GTY transceivers to support PCIe ×4 and PCIe ×1. FMC2: Provides 2 GTY transceivers to support PCIe ×1. 	-

See also

4.1 Delivery list

2.3.3 Rear view

The following figure and table explain the components at the rear of the UV APS.

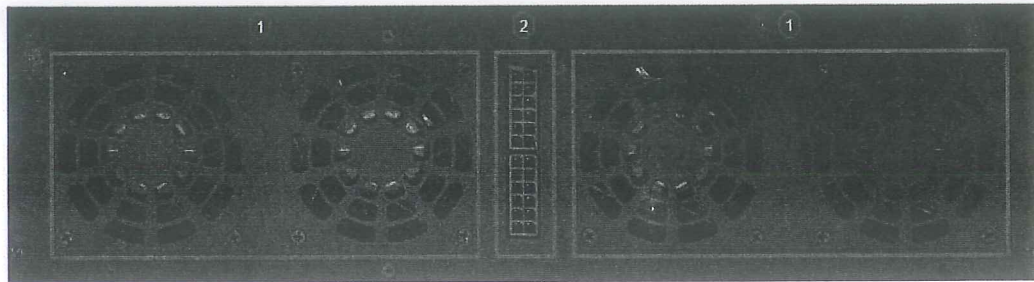


Figure 2-5 UV APS rear view

Table 2-3 Components at rear

Callout	Description	Connection cable
1	Four system cooling fans	-
2	<p>Power connectors</p> <p>Connects with an external power module UV-Desk-Pow to provide 12V into the UV APS.</p> <p>Note: The UV-Desk-Pow module contains a network power switch to enable remotely powering on/off the UV APS over Ethernet.</p>	<p>The power module UV-Desk-Pow also includes one AC and one DC cables.</p>

See also

4 Installation, commissioning, and maintenance

2.4 Technical data

Table 2-4 lists the physical and electrical specifications of the UV APS.

Table 2-4 General specifications of the UV APS

Item	Description
Prototyping FPGA	4 × Xilinx Virtex UltraScale+ XCVU19Ps
Power supply	12V V _{DC}
Power	Max. 1 kW per UV APS
Global clocks ¹	20 programable global clocks in the following ranges: <ul style="list-style-type: none"> • GCLK0 to GCLK7: 100 Hz to 720 MHz • GCLK8 to GCLK15: 100 Hz to 250 MHz • GCLK16 to GCLK19: 200K Hz to 720 MHz Resolution: 1 KHz
Feedback clocks ^{1,2}	16 feedback clocks in the range of 100 Hz to 800 MHz Resolution: 1 KHz
Resets ¹	4 resets
Dimensions	A 3U rackmount case in the dimensions of 439 mm × 740 mm × 110.35 mm 
Weight	20 kg
Temperature	20 C to 25 C (60 F to 77 F)
Humidity	40% to 55%

1. For details of the clock and reset distributions, see *Section 3.3, Clock module*.

2. The feedback clock FB0 is for internal use only.

2.5 System software

Table 2-5 lists the software and operating system (OS) used with the UV APS.

Table 2-5 Software used with the UV APS

Item	Description
Compiler	UV APS Compiler, version 2022.10
Runtime	UV APS Run, version 2022.10
UniVista Debugger	UVD, version 2022.06.P3
OS	CentOS 7.8
Synthesis, placement, and routing	Xilinx® Vivado®, version 2021.2

3 Module description

This chapter introduces the internal modules of the UV APS.

This chapter contains the following sections:

- 3.1 *Power LEDs*
- 3.2 *Control module*
- 3.3 *Clock module*
- 3.4 *B2B cascading interface*
- 3.5 *Signal probing module*

3.1 Power LEDs

The four LEDs on the front panel indicate power and working status of the four XCVU19Ps respectively.

After the power button is pressed, the valid LED states include:

- OFF: Powered off.
- Solid green: Powered on without configuration.
- Blinking green (fast): Under configuration.
- Blinking green (slow): Configuration completes and in service.
- Solid amber: No detection of the XCVU19P.
- Blinking amber (fast): Lost or a weak connection to the XCVU19P.
- Solid red: Abnormal voltage.
- Blinking red (fast): Failure in FPGA configuration, such as the voltage and clock configurations.
- Blinking red (slow): Abnormal temperatures or abnormal cooling fans.

See also

2.3.1 Front view

4.2 Installing the UV APS

3.2 Control module

The control module sits on a dedicated FPGA to support communications between the host and the XCVU19Ps.

The control module serves:

- Communication with the host through the PCIe Gen3 ×8 port on the front panel.
- Access and configuration of the XCVU19Ps, including power, clock, and different interfaces shown in *Section 2.1, Block diagram*.
- Monitoring the temperature of each XCVU19P.
- Controlling the cooling fans.
- Connections between control boards of the cascaded UV APSES through connecting the **B2B<n>** connectors on the front panel.

3.3 Clock module

Figure 3-1 shows the clock architecture of the UV APS. The 20 global clocks and 16 feedback clocks go through a crosspoint switch to distribute 20 clocks locally and 20 clocks at the **CLK OUTn** ports to cascade the slave UV APSes.

When a UV APS serves as a slave, it chooses 20 clocks from the local clocks and the clocks fed from the **CLK INn** ports, then passes the selected 20 clocks to a fanout buffer to create four copies of the clocks. Then, distribute the four copies of the 20 clocks to the four XCVU19Ps respectively.

Note: Currently, the slave UV APS selects clocks from the **CLK INn** ports.

Table 3-1 shows the clock distribution between one-master-one-slave UV APSes.

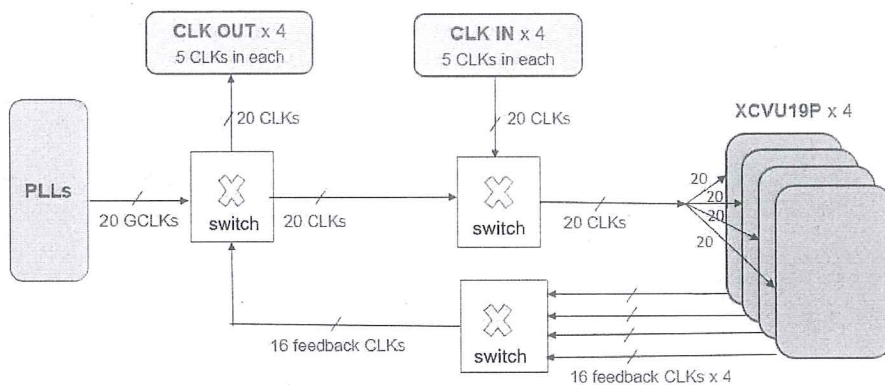


Figure 3-1 UV APS clock architecture

Table 3-1 Clock and reset distribution between 1:1 mater and slave

Master CLK OUT port	Slave CLK IN port	Transmitted clocks and resets
CLK OUT0	CLK IN0	Provides: <ul style="list-style-type: none"> 5 clocks, chosen from GCLK0 to GCLK4 and feedback clocks FB0 to FB3. Note: FB0 is used internally. 1 reset
CLK OUT1	CLK IN1	Provides: <ul style="list-style-type: none"> 5 clocks, chosen from GCLK5 to GCLK9 and feedback clocks FB4 to FB7. 1 reset
CLK OUT2	CLK IN2	Provides: <ul style="list-style-type: none"> 5 clocks, chosen from GCLK10 to GCLK14 and feedback clocks FB8 to FB11. 1 reset

Master CLK OUT port	Slave CLK IN port	Transmitted clocks and resets
CLK OUT3	CLK IN3	Provides: <ul style="list-style-type: none">• 5 clocks, chosen from GCLK15 to GCLK19 and feedback clocks FB12 to FB15.• 1 reset

For the location and description of the CLK OUT and CLK IN ports, see *Section 2.3.1, Front view*.

For the available frequency range, see *Section 2.4, Technical data*.

For system cascading, see *Section 3.4, B2B cascading interface*.

3.4 B2B cascading interface

The **B2B<n>** ports at the front panel serve to connect control modules of the cascaded UV APSes to transfer data in between.

The following table shows the connection between one master and one slave cascading.

Table 3-2 Connection between 1:1 master and slave

Master port	Slave port	Description
CLK OUT0 ¹	CLK IN0 ¹	Provide clock and reset connections between the cascaded UV APSes. For more details, see <i>Section 3.3, Clock module</i> .
CLK OUT1	CLK IN 1	
CLK OUT2	CLK IN 2	
CLK OUT3	CLK IN 3	
B2B<n> ²	B2B0 ²	Connect the control modules of the cascaded UV APSes.

1. The **CLK OUT0** to **CLK IN0** pair must be connected. The other clock pairs are optional depending on the number of clocks and resets to be used.
2. Currently, on the master UV APS any B2B port can be connected to the **B2B0** port on the slave. On the slave, only **B2B0** can be connected to.

For the location of the clock and B2B ports, see *Section 2.3.1, Front view*.

3.5 Signal probing module

The UV APS offers large, deep, and fast signal probing through the following components:

- The UV APS compiler tool, **UV APS Compiler**: Sets the trigger and probing signals.
- **Ultra-High Performance Debugger IPs (UHDs)**: Set triggering conditions on the trigger signals and capture cycle-based transitions of the probed signals.
- External DDR4 daughter cards: Store the captured waveform data from the mounted XCVU19Ps.
The UV APS offers four 16 GB DDR4 cards, UV-FMCH-PDDR4DME, to store the captured data. To use them with the signal probing module, fix each UV-FMCH-PDDR4DME to the **FMC3** connector on each XCVU19P.
- The UV APS runtime tool, **UV APS Run**: Transfers data from the UV APS to the host speedily and generates a USDB waveform database.
USDB is short for unified signal database. It is developed by UniVista to provide a more compact waveform format but with more debugging capabilities than the VCD format.
The USDB waveforms can be viewed only on the UniVista debugging tool, UniVista Debugger (UVD).
- The waveform debugging tool, **UniVista Debugger (UVD)**: Views and debugs signal waveforms easily with its intuitive graphical interface and the helpful debugging widgets on the UVD.

Among these components, the UHDs play the key role to capture large sets of signals at flexible combinations of different triggering conditions, including the combinations of >, >=, <, <=, ==, !=, failing edges, raising edges, any transition edges, no edge, OR, AND, and sequencing.

The features of the UHDs are:

- Inserted to the XCVU19Ps that contain the trigger and probing signals, which is automatically performed by the UV APS Compiler after having auto-partitioned the design.
- Each inserted XCVU19P supports up to 35 groups of probed signals. Such groups are called capture station hardware modules, instantiated by the UHDs.

The probed signal data width of each capture station is 512 bits.

- The whole UV APS system including the cascaded UV APSes supports up to 16 groups of trigger signals. Such groups are called trigger group hardware modules, instantiated by the UHDs.

The trigger signal data width of each trigger group is 256 bits and they must share the same clock domain.

- Each trigger group can divide the contained trigger signals up to 16 subsets to provide up to 16 different trigger conditions, including >, >=, <, <=, ==, !=, failing edges, raising edges, any transition edges, no edge, OR, AND, and a sequential ordering.
- Trigger groups of the same clock domain can be conditioned by OR, AND, or ordered in a sequence.
- Trigger groups of different clock domains are independent from each other.

- All trigger groups and capture stations are enabled at runtime by the UV APS Run and share the 20 clock domains on the UV APS.
- Storing the captured data to DDR and controlling the DDR access from the host.

4 Installation, commissioning, and maintenance

This chapter describes installation, commissioning, and maintenance of the UV APS.

This chapter contains the following sections:

- *4.1 Delivery list*
- *4.2 Installing the UV APS*
- *4.3 Commissioning of the UV APS*
- *4.4 Troubleshooting*

4.1 Delivery list

On receiving the UV APS, carefully remove the package and check the contained items against the received delivery list. If any item is missing, mismatched, or damaged, contact your UniVista support engineers.

Table 4-1 lists the delivery list for full interconnections on the UV APS. Your received delivery list may vary from this list if you choose partial interconnections or order additional daughter cards, cables, or others.

Table 4-1 UV APS full interconnection delivery list

Item	QTY	Part No.	Note
UV APS system	1	-	Includes both the UV APS hardware and the software package. The software contains: <ul style="list-style-type: none"> • Compiler: UV APS Compiler • Runtime: UV APS Run • Debugger: UniVista Debugger
Desktop power module	1	UV-Desk-Pow	This module supplies power to the UV APS and converts the input AC voltage to 12V DC voltage to the UV APS. Along with this module, one AC and one DC cables are provided. This module also contains a network power switch to enable remotely powering on/off the UV APS over Ethernet.
Ethernet cable	1	-	Standard Connects to <u>the ETH connector</u> used for system upgrade.
PCIe host communication card	1	UV-SASX8-PCIE	<ul style="list-style-type: none"> • On the host, install the card UV-SASX8-PCIE. • On the UV APS, connect <u>the PICEX8 connector</u> to the UV-SASX8-PCIE card with the provided 1-meter cable, UV-IOC-1000.
DDR4 daughter card	4	UV-FMCH-PDDR4DME	16 GB SODIMM DDR4, 72-bit data width single rank, 2666 MT/s, ECC supported When they are used with the <u>signal probing module</u> , fix each card to the FMC3 connector on each XCVU19P.

Item	QTY	Part No.	Note
Daughter cards to convert from FMC connectors to the high performance IO connectors, IOC connectors	16	UV-FMCH-OBU1 ¹	Each card provides three IOC connectors, IOC0 to IOC2 . When connecting IOC connectors between different UV-FMCH-OBU1 cards, match the connectors of the same indexes.
Daughter cards to convert from APC to IOC connectors Note: These cards apply to APC0 to APC11 connectors.	16	UV-OBO-SAS ¹	Each card provides three IOC connectors, IOC0 to IOC2 to match three APCs from APC0 to APC11 . Note: APC<n> to APC<n+2> use one UV-OBO-SAS, where n = 0, 3, 6, and 9.
Daughter cards to convert from APC to IOC connectors Note: These cards apply to APC12 to APC23 connectors.	16	UV-OBM-SAS ¹	Each card provides three IO connectors, IOC0 to IOC2 to match three APCs from APC12 to APC23 . Note: APC<n> to APC<n+2> use one UV-OBM-SAS, where n = 12, 15, 18, and 21.
Interconnection cables between IOC connectors	72	UV-IOC-500 ¹	Length: 50 cm
Interconnection cables between HGC connectors	16	UV-HGC-1000 ¹	Length: 1m

1. These items are provided on demand.

4.2 Installing the UV APS

This section describes the UV APS physical installation and connection to the host.

Note: Only qualified personnel can install the UV APS.

Prerequisites

Make sure:

- Read through the safety instructions provided in *Chapter 1, Safety*.
- Carefully check the received package as described in *Section 4.1, Delivery list*.
- The installation location is clean and provides sufficient space to accommodate the mounting hardware including the UV APS system case, cables, and power module.

For the physical measurement data of the UV APS, see *Section 2.4, Technical data*.

- The installation location is well-ventilated to allow air flow for proper operation of the UV APS.
- The host PC is powered off.
- The host PC has already installed the UV APS software package and all other companion tools listed in *Section 2.5, System software*.

Procedure

WARNING!

- To avoid system damages from electrostatic discharge (ESD), always wear a static protection wrist strap while performing any procedures that require physically contact with the UV APS system, including connection of cables, daughter cards, and power supply.
- To safely operate the system, always power off the UV APS before performing any procedures that require physically contact with the UV APS system, including connection of cables, daughter cards, and power supply.

1. Carefully place the UV APS into the installation location.
2. Carefully fit the four provided 16GB DDR4 daughter cards, UV-FMCH-PDDR4DME, to the UV APS.

During fitting:

- Install one DDR4 card to one XCVU19P at the **FMC3** connector.
The DDR4 cards will store the captured signals at runtime.
 - Keep the card parallel to the UV APS to avoid any damage to socket pins or other components.
3. (Optional) Carefully fit the other needed daughter cards to the FMC connectors on the UV APS.
 4. Work with the UniVista support engineers to interconnect the four XCVU19Ps on the UV APS.

5. Connect the UV APS to the host PC as follows:
 - a. On the host PC, install the provided PCIe 8-lane daughter card UV-SASX8-PCIE.
 - b. On the UV APS, use the provided cable UV-IOC-*<length_mm>* to connect the front panel connector **PCIEX8** to the UV-SASX8-PCIE card.
6. Connect the power supply to the UV APS as follows:
 - a. Fit the DC and AC cables to the power module UV-Desk-Pow.
 - b. Connect the AC cable to the power supply.
 - c. Connect the DC cable to the power connectors at the rear of the UV APS.
 - d. Use an Ethernet cable to connect the UV-Desk-Pow to the network hub that connects to the host PC.

This connection serves remote power-on and power-off of the UV APS.

7. Power on the UV APS by pressing the power button on the front panel.
8. Wait until the four power LEDs are solid green.

If the LEDs are off or solid amber, power off the UV APS immediately, and then contact your UniVista support engineers, as which indicates the XCVU19Ps lose detections.

For details of the LED indications, see *Section 3.2, Power status LEDs*.

9. Power up the host PC.

Result

The UV APS successfully connects to the host.

What to do next

Test the connections at connectors and daughter cards as described in *Section 4.3, Commissioning of the UV APS*.

4.3 Commissioning of the UV APS

This section describes the procedures to test different connections at the UV APS, including the connectors and fitted daughter cards.

About this task

After installation of the UV APS or a daughter card, run the diagnostic scripts on the runtime software UV APS Run to examine:

- Connections at connectors
- Temperature, voltage, and the fan speed of each XCVU19P
- Working status of each XCVU19P

Prerequisites

Make sure the UV APS including the software package is well installed as described in *Section 4.2, Installing the UV APS*.

Procedure

WARNING!

- To avoid system damages from electrostatic discharge (ESD), always wear a static protection wrist strap while performing any procedures that require physically contact with the UV APS system, including connections of cables, daughter cards, and power supply.
- To safely operate the system, always power off the UV APS before performing any procedures that require physically contact with the UV APS system, including connections of cables, daughter cards, and power supply.

1. (Optional) Carefully fit the needed daughter cards to the FMC connectors on the UV APS.
2. Log on to the host that connects to the UV APS system.
3. Link the directory `<uvaps_SW_install_dir>/platform/U2/diagnostic` to your local directory.
4. Follow the README file here to diagnose the connections at connectors.
5. If daughter cards are connected, obtain the card diagnostic instructions and scripts from the UniVista support engineers.

Troubleshooting

After you run the design on the UV APS with the runtime software UV APS Run, the UV APS Run starts monitoring the UV APS and reports the status on the terminal:

- If you see alarms, system warnings, or severe errors, take immediate actions by strictly following the on-screen instructions.
- For normal errors or warnings reported at command executions, troubleshoot the issues against the on-screen prompts or check the log files for possible reasons.

Note: If the issue persists, contact the UniVista support engineers.

5 Performing prototyping

This chapter outlines the prototyping workflow on the UV APS. For detailed procedures and command descriptions, see *UV APS Software User Guide*.

The chapter contains the following section:

- 5.1 Prototyping workflow on the UV APS

5.1 Prototyping workflow on the UV APS

Use the provided UV APS software to perform prototyping verifications on the UV APS.

The software includes:

- **UV APS Compiler:** Compiles and partitions your design automatically.
- **UV APS Run:** Controls and manages the XCVU19Ps at runtime including voltage and clock configurations, downloading the compiled bitstreams, querying status from the XCVU19Ps, and capturing the probed signals.
- **UniVista Debugger (UVD):** Views and debugs the waveforms of the captured signals.

Prerequisites

Make sure:

- The UV APS is successfully installed as described in *Section 4.2, Installing the UV APS* and *Section 4.3, Commissioning of the UV APS*.
- Log on to the host that connects to the UV APS.

Procedure

WARNING!

- To avoid system damages from electrostatic discharge (ESD), always wear a static protection wrist strap while performing any procedures that require physically contact with the UV APS system, including connections of cables, daughter cards, and power supply.
- To safely operate the system, always power off the UV APS before performing any procedures that require physically contact with the UV APS system, including connections of cables, daughter cards, and power supply.

1. From the host, compile your design with the **UV APS compiler**.
2. Use the runtime software **UV APS Run** to configure, download, and run the compiled design on the XCVU19Ps of the UV APS.
3. Use the **UV APS Run** to capture the probed signals and store them into the provided DDR4 daughter cards, UV-FMCH-PDDR4DME.

For features about the signal probing on the UV APS, see *Section 3.5, Signal probing module*.

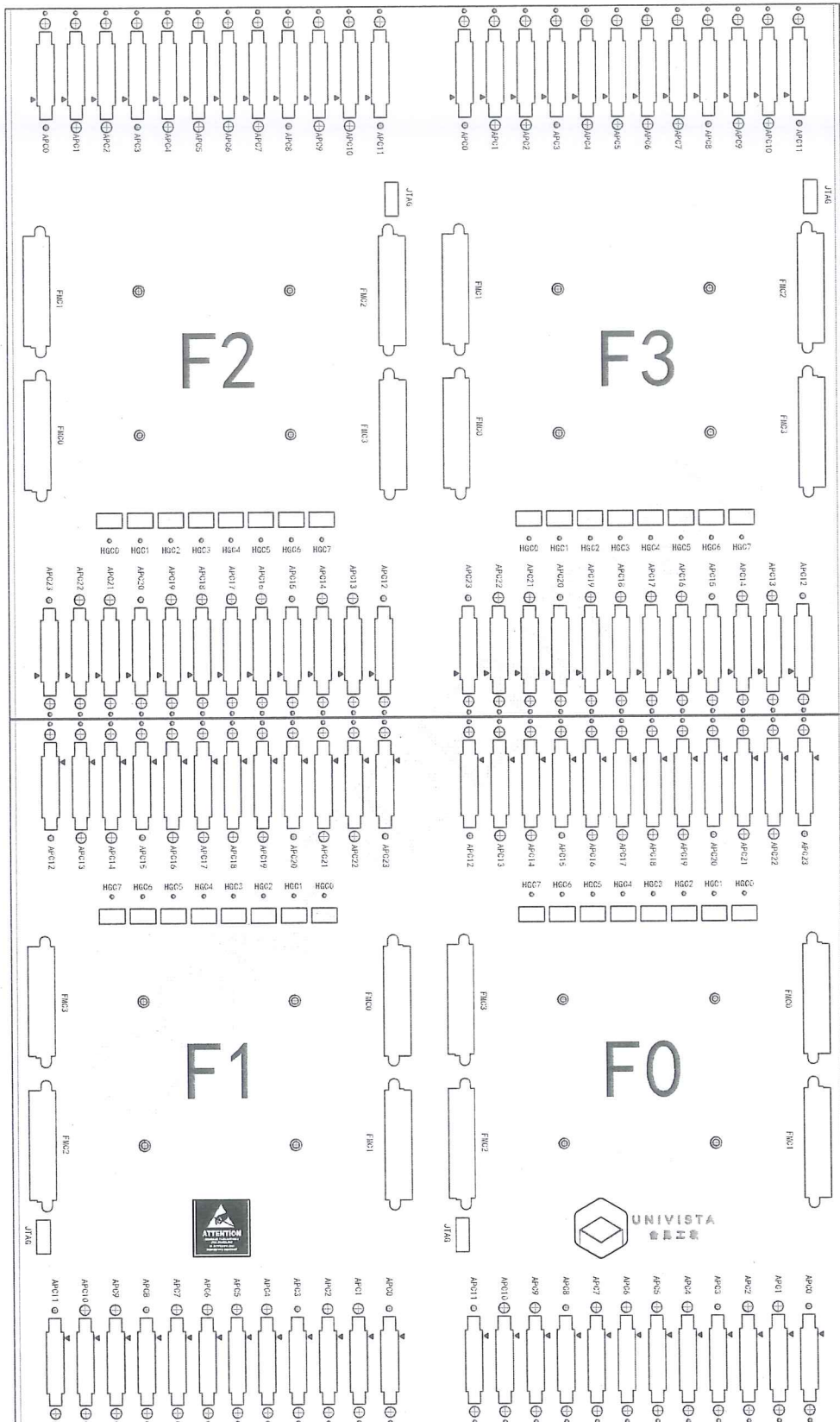
4. Use the UVD to view and debug the waveforms of the captured signals.

Note: For procedures to use the UV APS Compiler and UV APS Run, see the *UV APS Software User Guide*.

A Appendix A: UV APS drawings

This appendix includes detailed drawings of the UV APS:

- Top view of the UV APS



B Appendix B: FMC pin list

Each XCVU19P on the UV APS provides four high-pin count (HPC) FMC connectors. Each FMC connector provides 149 IOs listed in Table B-1.

Table B-1 149 FMC IO pins in use

FMC pin number	FMC pin name	FMC pin index
C10	LA06_P	89
C11	LA06_N	90
C14	LA10_P	93
C15	LA10_N	94
C18	LA14_P	97
C19	LA14_N	98
C22	LA18_P_CC	101
C23	LA18_N_CC	102
C26	LA27_P	105
C27	LA27_N	106
D8	LA01_P_CC	127
D9	LA01_N_CC	128
D11	LA05_P	130
D12	LA05_N	131
D14	LA09_P	133
D15	LA09_N	134
D17	LA13_P	136
D18	LA13_N	137
D20	LA17_P_CC	139
D21	LA17_N_CC	140
D23	LA23_P	142
D24	LA23_N	143
D26	LA26_P	145
D27	LA26_N	146
E2	HA01_P_CC	161
E3	HA01_N_CC	162
E6	HA05_P	165
E7	HA05_N	166
E9	HA09_P	168
E10	HA09_N	169
E12	HA13_P	171

FMC pin number	FMC pin name	FMC pin index
E13	HA13_N	172
E15	HA16_P	174
E16	HA16_N	175
E18	HA20_P	177
E19	HA20_N	178
E21	HB03_P	180
E22	HB03_N	181
E24	HB05_P	183
E25	HB05_N	184
E27	HB09_P	186
E28	HB09_N	187
F4	HA00_P_CC	203
F5	HA00_N_CC	204
F7	HA04_P	206
F8	HA04_N	207
F10	HA08_P	209
F11	HA08_N	210
F13	HA12_P	212
F14	HA12_N	213
F16	HA15_P	215
F17	HA15_N	216
F19	HA19_P	218
F20	HA19_N	219
F22	HB02_P	221
F23	HB02_N	222
F25	HB04_P	224
F26	HB04_N	225
F28	HB08_P	227
F29	HB08_N	228
F31	HB12_P	230
G2	CLK1_M2C_P	241
G3	CLK1_M2C_N	242
G6	LA00_P_CC	245
G7	LA00_N_CC	246
G9	LA03_P	248
G10	LA03_N	249
G12	LA08_P	251
G13	LA08_N	252

FMC pin number	FMC pin name	FMC pin index
G15	LA12_P	254
G16	LA12_N	255
G18	LA16_P	257
G19	LA16_N	258
G21	LA20_P	260
G22	LA20_N	261
G24	LA22_P	263
G25	LA22_N	264
G27	LA25_P	266
G28	LA25_N	267
G30	LA29_P	269
G31	LA29_N	270
G33	LA31_P	272
G34	LA31_N	273
G36	LA33_P	275
G37	LA33_N	276
H4	CLK0_M2C_P	283
H5	CLK0_M2C_N	284
H7	LA02_P	286
H8	LA02_N	287
H10	LA04_P	289
H11	LA04_N	290
H13	LA07_P	292
H14	LA07_N	293
H16	LA11_P	295
H17	LA11_N	296
H19	LA15_P	298
H20	LA15_N	299
H22	LA19_P	301
H23	LA19_N	302
H25	LA21_P	304
H26	LA21_N	305
H28	LA24_P	307
H29	LA24_N	308
H31	LA28_P	310
H32	LA28_N	311
H34	LA30_P	313
H35	LA30_N	314

FMC pin number	FMC pin name	FMC pin index
H37	LA32_P	316
H38	LA32_N	317
J2	CLK3_BIDIR_P	321
J3	CLK3_BIDIR_N	322
J6	HA03_P	325
J7	HA03_N	326
J9	HA07_P	328
J10	HA07_N	329
J12	HA11_P	331
J13	HA11_N	332
J15	HA14_P	334
J16	HA14_N	335
J18	HA18_P	337
J19	HA18_N	338
J21	HA22_P	340
J22	HA22_N	341
J24	HB01_P	343
J25	HB01_N	344
J27	HB07_P	346
J28	HB07_N	347
J30	HB11_P	349
J31	HB11_N	350
K4	CLK2_BIDIR_P	363
K5	CLK2_BIDIR_N	364
K7	HA02_P	366
K8	HA02_N	367
K10	HA06_P	369
K11	HA06_N	370
K13	HA10_P	372
K14	HA10_N	373
K16	HA17_P_CC	375
K17	HA17_N_CC	376
K19	HA21_P	378
K20	HA21_N	379
K22	HA23_P	381
K23	HA23_N	382
K25	HB00_P_CC	384
K26	HB00_N_CC	385

FMC pin number	FMC pin name	FMC pin index
K28	HB06_P_CC	387
K29	HB06_N_CC	388
K31	HB10_P	390
K32	HB10_N	391



合见工软
UNIVISTA

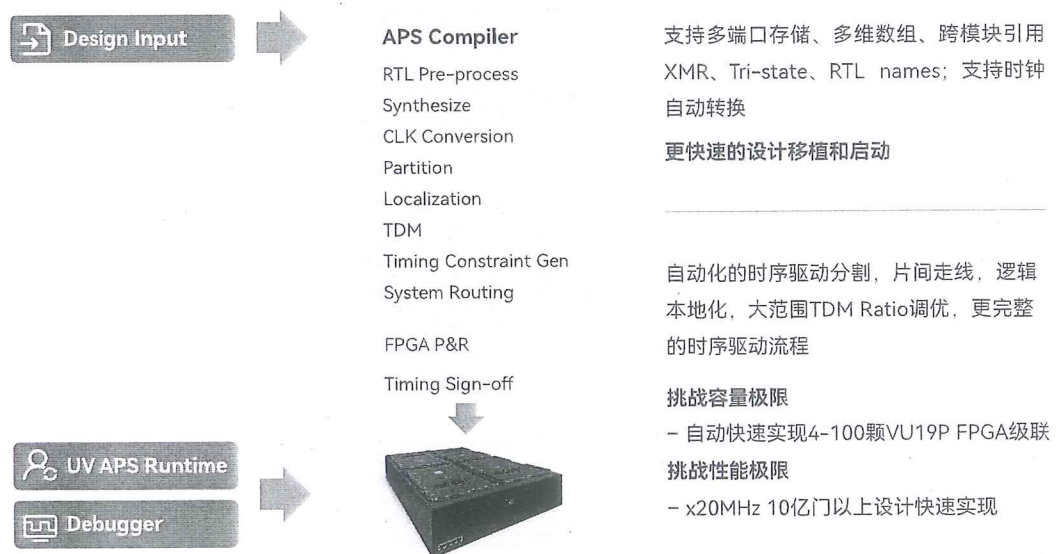
UniVista Advanced Prototyping System

先进FPGA原型验证系统

产品介绍

上海合见工业软件集团有限公司（简称“合见工软”）推出灵活、可扩展的先进FPGA原型验证系统UniVista Advanced Prototyping System（简称“UV APS”）。UV APS适用于大规模ASIC原型验证及SoC的开发，单套设备使用了4片Xilinx VU19P FPGA，可灵活堆叠，最大容量支持25套设备级联（100片FPGA互联）。集成智能化、自动化的全流程编译软件 APS Compiler为芯片设计者提供了高效的验证方式，降低在验证阶段的时间成本；同时提供丰富的FMC接口子卡，以适配各种接口验证，提供充足的One-Bank互联通道，以支撑系统扩展；配合深度调试方案，缩短测试周期，加快芯片上市。

UV APS 自动化时序驱动编译流程



性能优势

- 适用于SoC芯片验证的卓越编译性能，高达20+MHz；相较VU440，速度提升近1.5倍
- 支持时序驱动的多片分割
- 支持虚拟原型和FPGA原型系统的混合验证

- 提供面向多种垂直行业应用的子卡及快速定制服务
- 自动化回归管理集成及企业级云部署，可靠、安全，高效管理资源

规格特征

高性能、自动化编译流程

- 时序驱动的分割引擎，并支持手动分割向导
- 时序驱动的逻辑本地化，优化分割的FPGA网表，具有更好的预P&R系统级时序
- 门控时钟自动转换
- 大范围TDM Ratio (1: 1024) 自动最优求解
- 支持多端口多维数组自动映射片内或者片外存储资源

多样化调试手段

- 回读捕获 (Readback Capture) 调试，可读取片内寄存器值
- 超宽信号采集与深度存储调试

大容量

- Xilinx Virtex UltraScale Plus VU19P FPGA，最大容量支持100片FPGA互联

丰富的可扩展接口

- 单颗FPGA提供1700+用户IO，支撑充足的信号互联
- FMC连接器，可扩展标准FMC接口子卡
- 28Gbps高速收发器

多路可编程全局时钟

Runtime软件

- 支持上位机软件控制，包括配置、下载、运行和调试
- 提供命令行的交互方式，支持TCL脚本语言

系统自检测

系统安全

- 系统状态/温度监测
- 过压/过流保护